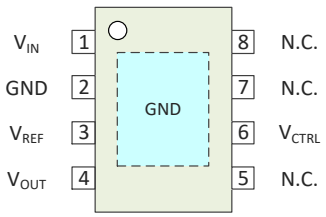
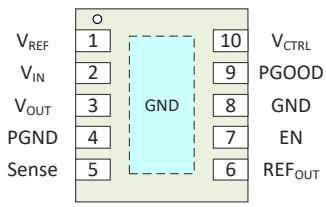
DDR Bus Termination Regulator

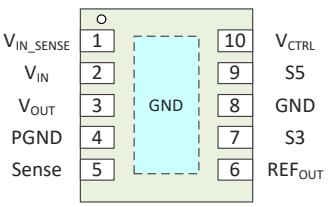
- Solution for DDR bus SSTL (Series Stub Termination Logic) termination for DDRI ~ DDRIV
  - ❑ DDRIV: 1.2V ❑ DDRIIIL:1.35V
  - ❑ DDRIII: 1.5V ❑ DDRII: 1.8V
  - ❑ DDRI: 2.5V
- Regulates DDR bus voltage for signal integrity
- Multiple control options: EN, S3/S5, PowerGood pins for power sequence control.
- Tiny packages MSOP, DFN3x3 for compact design



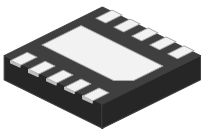
UR6517



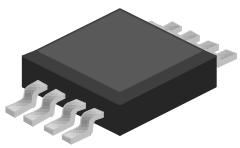
UR5513



UR5517



DFN3030-10



MSOP-8

Part NO.	Package	DDR support & control function
UR6517	HSOP	DDR4 & DDR3L (1.2A) DDR3 (1.5A) DDR2&1 (1.8A)
UR5513	DFN3030 MSOP	DDR4~DDR3 (2A), EN, PoR control
UR5517	DFN3030 (H)MSOP	DDR3 (2A), S3/S5 control
UR6511	(H)SOP	DDR3LP~DDR1 (3A)
UR6515D	HSOP	DDR3 (3A)
UR6512 UR6515C	HSOP	DDR3 (2A)
Others		1.5~3A, EN, Sense

Global Business Group, Unisonic Technologies Co., Ltd
- Tel: +886-2-2999 5013 ext .218
- e-Mail : oversea@unisonic.com.tw