

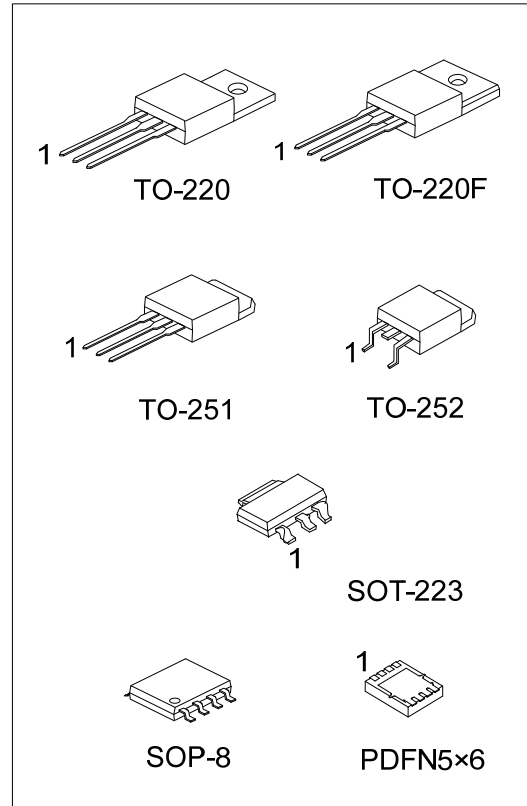
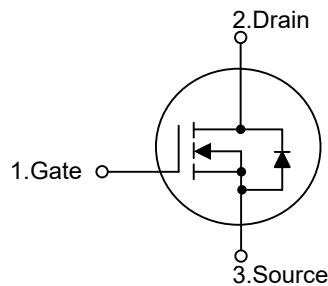
**2N60-LC1****Power MOSFET****2.0A, 600V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **2N60-LC1** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **2N60-LC1** is generally applied in low power switching mode power appliances and electronic ballast.

FEATURES

- * $R_{DS(ON)} \leq 5.0 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
2N60L-AA3-R	2N60G-AA3-R	SOT-223	G	D	S	-	-	-	-	-	Tape Reel
2N60L-TA3-T	2N60G-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
2N60L-TF3-T	2N60G-TF3-T	TO-220F	G	D	S	-	-	-	-	-	Tube
2N60L-TM3-T	2N60G-TM3-T	TO-251	G	D	S	-	-	-	-	-	Tube
2N60L-TN3-R	2N60G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
2N60L-S08-R	2N60G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
2N60L-P5060-R	2N60G-P5060-R	PDFN5x6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

	(1)Packing Type	(1) R: Tape Reel, T: Tube
	(2)Package Type	(2) AA3: SOT-223, TA3: TO-220, TF3: TO-220F TM3: TO-251, TN3: TO-252, S08: SOP-8 P5060: PDFN5x6
	(3)Green Package	(3) G: Halogen Free and Lead Free, , L: Lead Free

MARKING

SOT-223	TO-220 / TO-220F / TO-251 / TO-252
The diagram shows a rectangular package with a notch on the left. The marking '2N60' is in the top right, 'LC1' is in the bottom left, and four empty boxes are in the bottom right. Arrows point from '2N60' to 'L: Lead Free' and 'G: Halogen Free', and from 'LC1' to 'Date Code'. A 'Version Code' arrow points to the left. A '1' is at the bottom left.	The diagram shows a package with a notch on the left. The marking 'UTC' is in the top right, '2N60' is in the middle right, 'LC1' is in the bottom left, and four empty boxes are in the bottom right. Arrows point from '2N60' to 'L: Lead Free' and 'G: Halogen Free', and from 'LC1' to 'Date Code'. 'Version Code' and 'Lot Code' arrows point to the left. A '1' is at the bottom left.
SOP-8	PDFN5x6
The diagram shows an 8-pin package. The marking 'UTT' is in the top left, '2N60' is in the middle right, 'LC1' is in the bottom left, and four empty boxes are in the bottom right. Arrows point from '2N60' to 'L: Lead Free' and 'G: Halogen Free', and from 'LC1' to 'Lot Code'. 'Date Code' and 'Version Code' arrows point to the left. Pins are numbered 1-8.	The diagram shows a package with a notch on the left. The marking 'UTC' is in the top right, '2N60' is in the middle right, and 'LC1' followed by four empty boxes is in the bottom right. Arrows point from '2N60' to 'L: Lead Free' and 'G: Halogen Free', and from 'LC1' to 'Date Code'. 'Version Code' and 'Date Code' arrows point to the left.

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	600	V
Gate-Source Voltage		V _{GSS}	±30	V
Drain Current	Continuous	I _D	2	A
	Pulsed (Note 2)	I _{DM}	4	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	33.8	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.6	V/ns
Power Dissipation	SOT-223	P _D	2.3	W
	TO-220		54	W
	TO-220F		20	W
	TO-251/TO-252		45	W
	SOP-8		2	W
	PDFN5×6		20	W
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L = 10mH, I_{AS} = 2.6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

4. I_{SD} ≤ 2.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ _{JA}	160	°C/W
	TO-220/TO-220F		62.5	°C/W
	TO-251/TO-252		100	°C/W
	SOP-8		190	°C/W
	PDFN5×6		65(Note)	°C/W
Junction to Case	SOT-223	θ _{JC}	54 (Note)	°C/W
	TO-220		2.32	°C/W
	TO-220F		6.25	°C/W
	TO-251/TO-252		2.77 (Note)	°C/W
	SOP-8		62.5 (Note)	°C/W
	PDFN5×6		6.25 (Note)	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

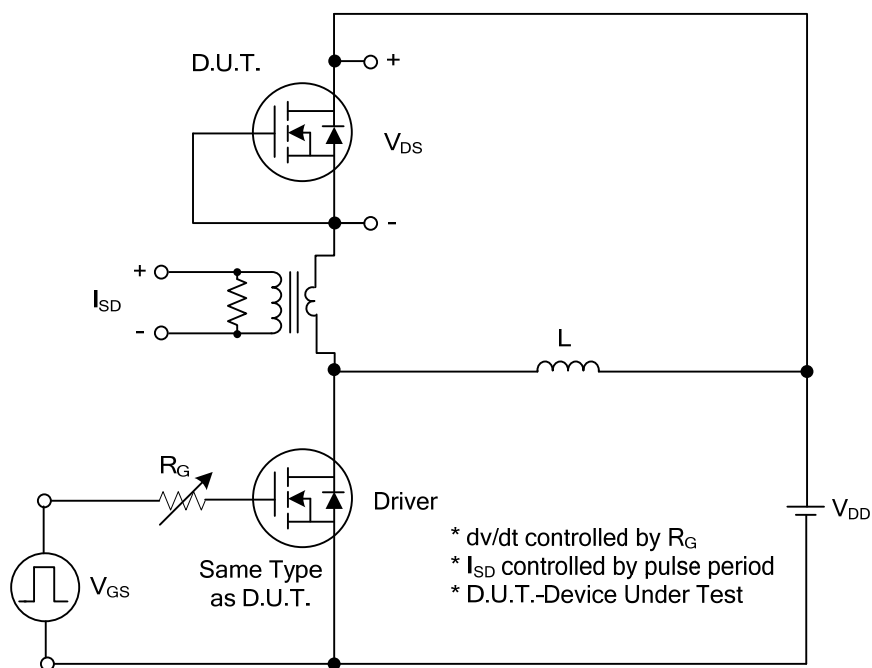
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	600			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =600V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			5.0	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		285		pF
Output Capacitance		C _{OSS}			30		pF
Reverse Transfer Capacitance		C _{RSS}			2.3		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =480V, V _{GS} =10V, I _D =2.0A I _G =1mA (Note 1, 2)		7		nC
Gate to Source Charge		Q _{GS}			2.9		nC
Gate to Drain Charge		Q _{GD}			0.9		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =2.0A, R _G =25Ω (Note 1, 2)		4		ns
Rise Time		t _R			14.5		ns
Turn-OFF Delay Time		t _{D(OFF)}			16		ns
Fall-Time		t _F			23.5		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				2	A
Maximum Body-Diode Pulsed Current (Note 1)		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =2.0A, V _{GS} =0V,		285		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dl _F /dt=100A/μs		1		μC

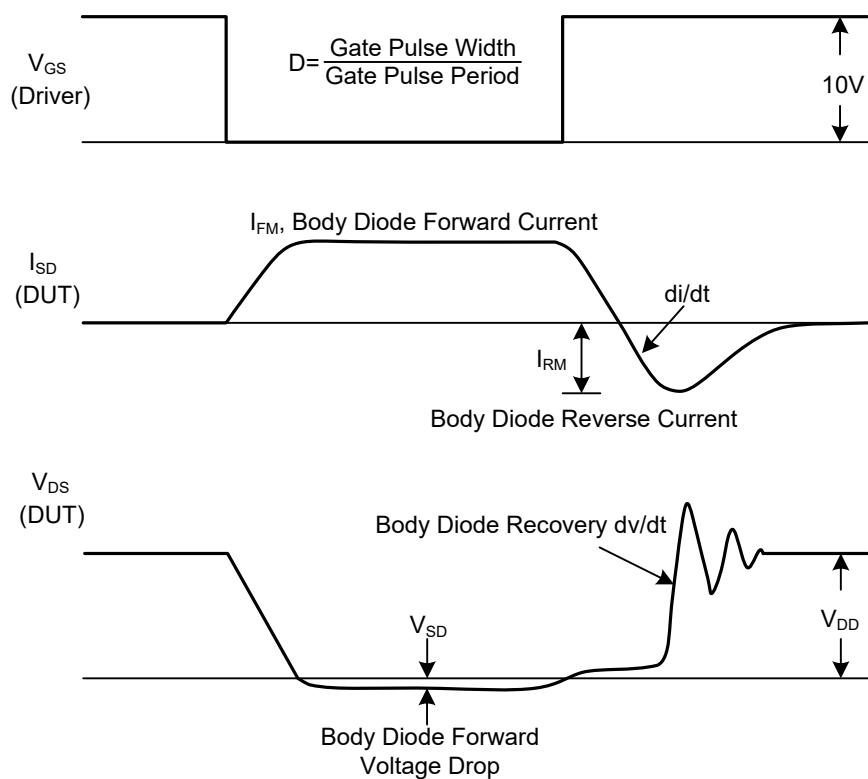
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

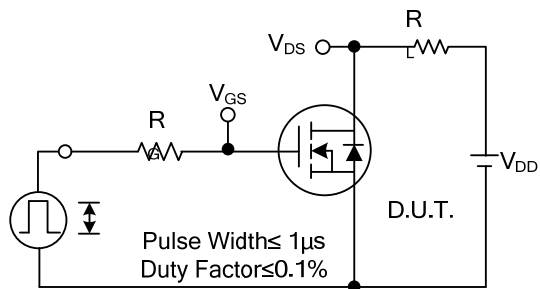


Peak Diode Recovery dv/dt Test Circuit

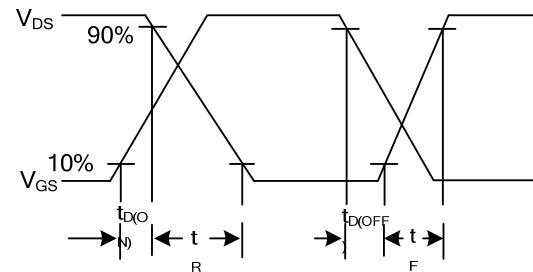


Peak Diode Recovery dv/dt Waveforms

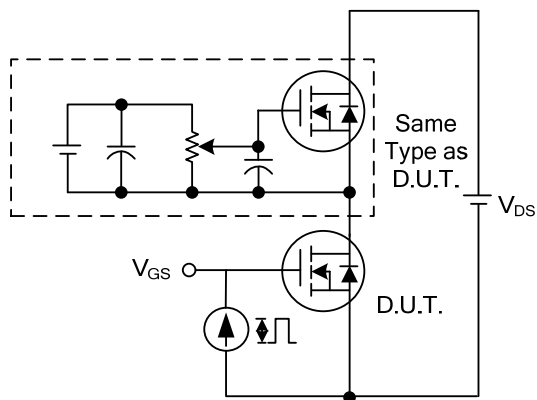
■ TEST CIRCUITS AND WAVEFORMS



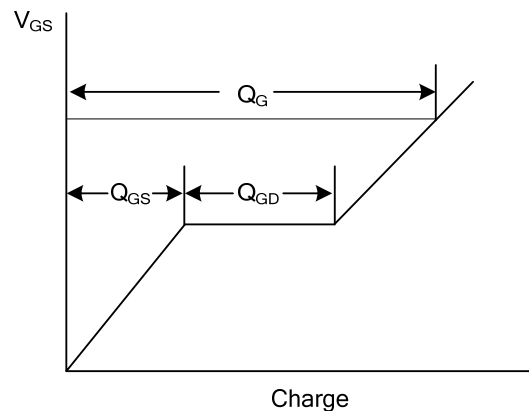
Switching Test Circuit



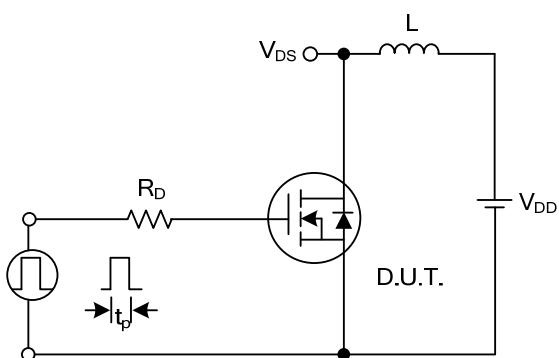
Switching Waveforms



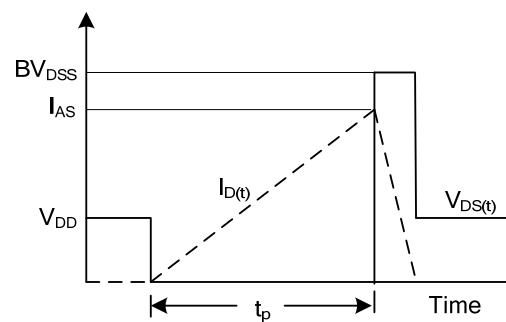
Gate Charge Test Circuit



Gate Charge Waveform

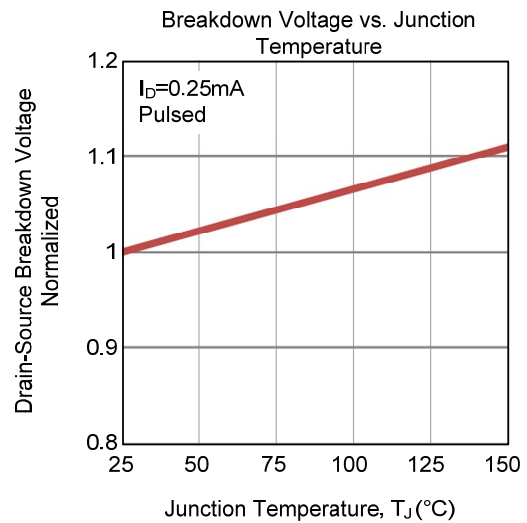
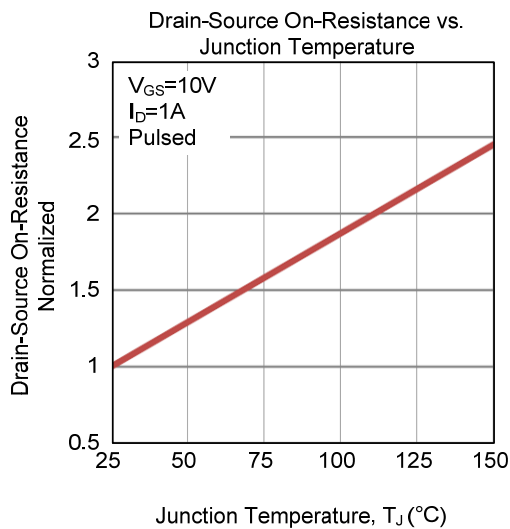
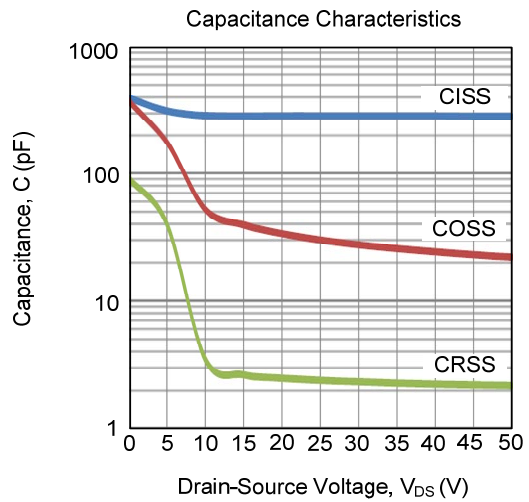
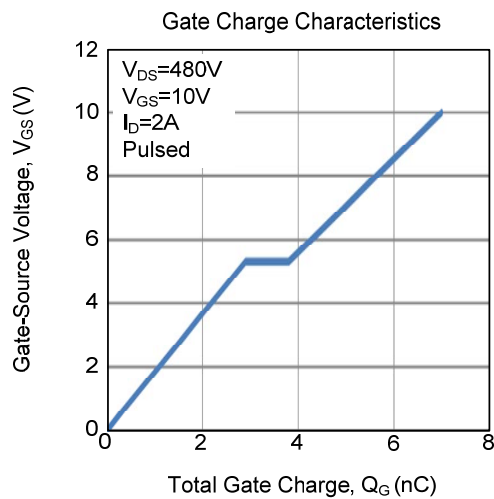
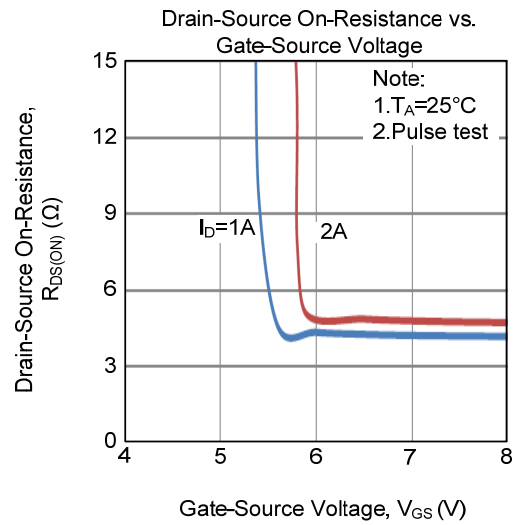
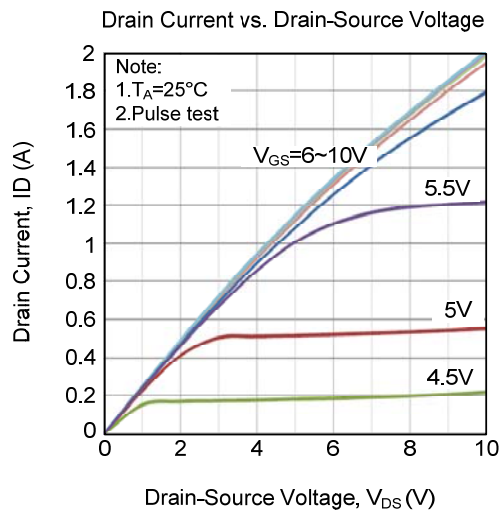


Unclamped Inductive Switching Test Circuit

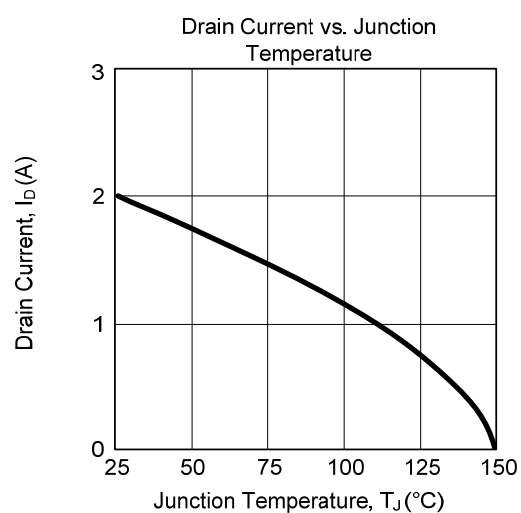
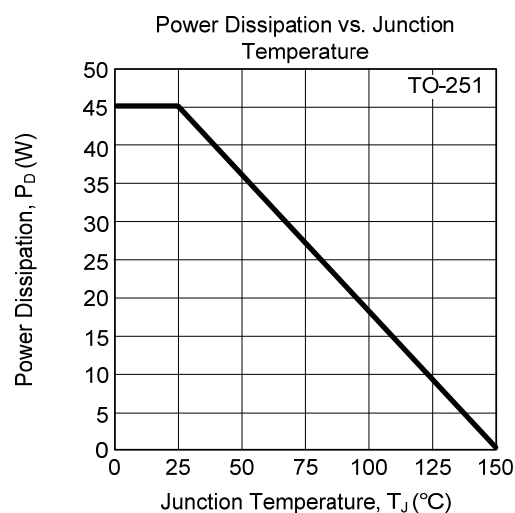
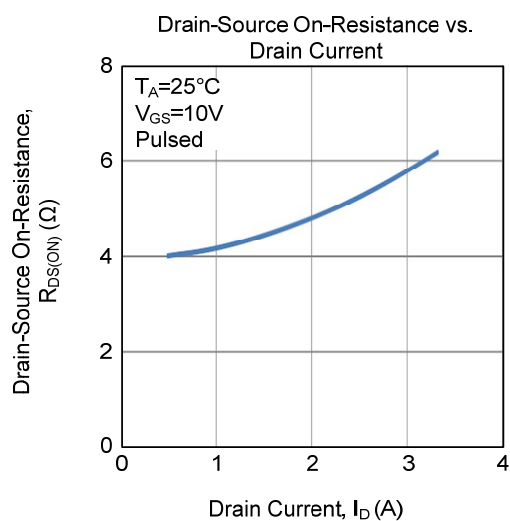
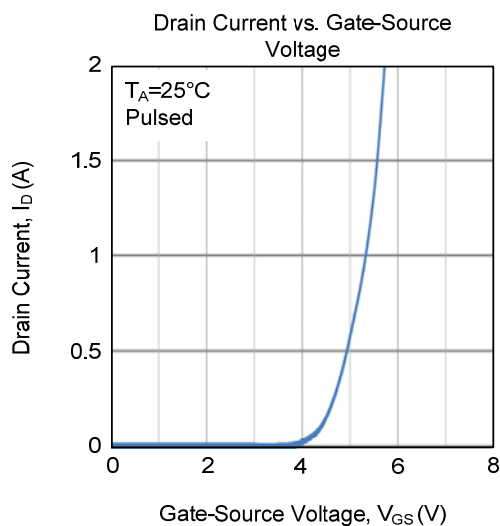
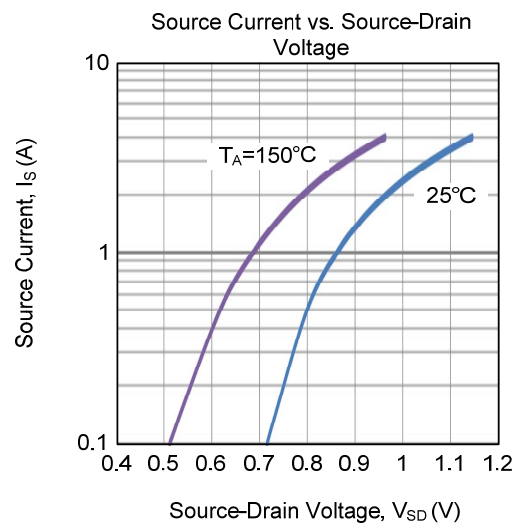
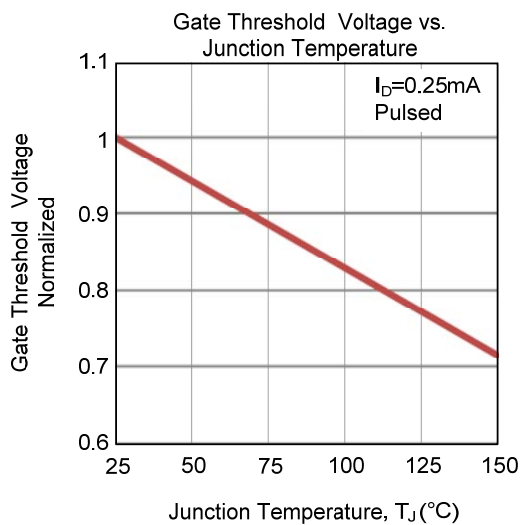


Unclamped Inductive Switching Waveforms

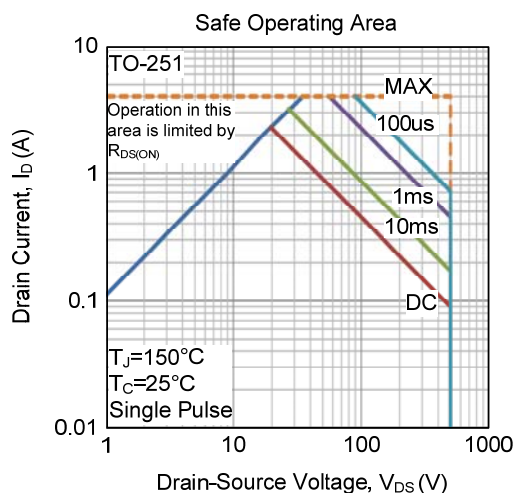
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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