



2N70A-LC1

Power MOSFET

2A, 700V N-CHANNEL POWER MOSFET

DESCRIPTION

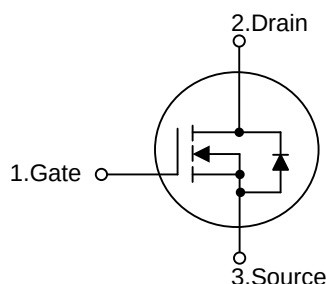
The UTC **2N70A-LC1** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

The UTC **2N70A-LC1** is generally applied in low power switching mode power appliances and electronic ballast.

FEATURES

- * $R_{DS(ON)} \leq 8.5 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



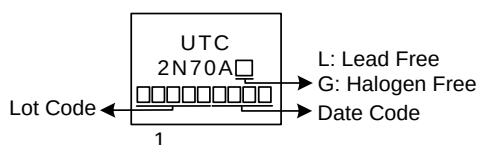
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N70AL-TM3-T	2N70AG-TM3-T	TO-251	G	D	S	Tube
2N70AL-TN3-R	2N70AG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

2N70AG-TM3-T		(1) Packing Type	(1) T: Tube, R: Tape Reel
		(2) Package Type	(2) TM3: TO-251, TN3: TO-252
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	2	A
	Pulsed (Note 2)	I_{DM}	4	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	38.4	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.1	V/ns
Power Dissipation		P_D	40	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 1.6\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	100	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.125 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

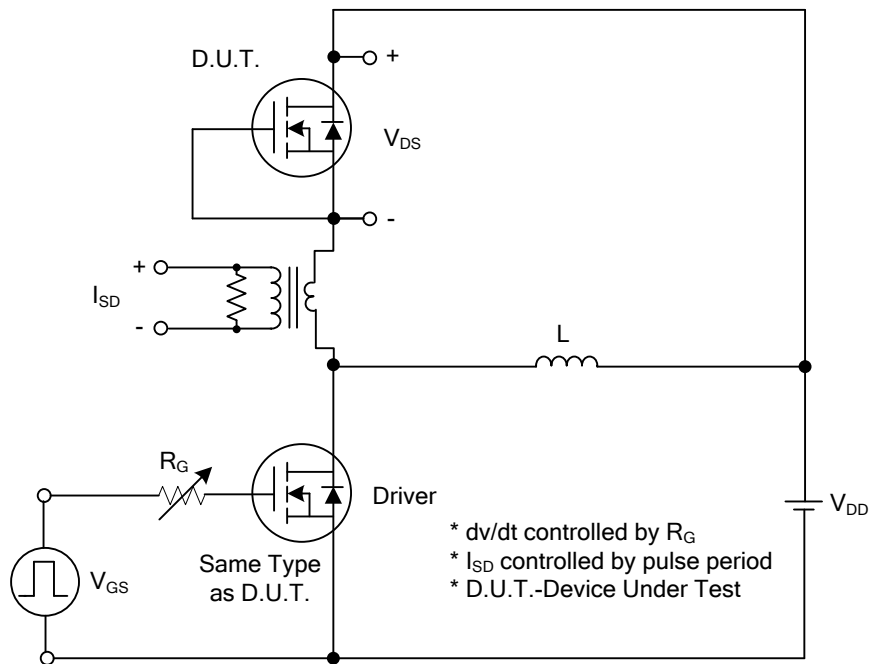
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	700			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =700V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			8.5	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		225		pF
Output Capacitance		C _{OSS}			26		pF
Reverse Transfer Capacitance		C _{RSS}			2.8		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =560V, V _{GS} =10V, I _D =2A I _G =1mA (Note 1, 2)		6.8		nC
Gate to Source Charge		Q _{GS}			2.7		nC
Gate to Drain Charge		Q _{GD}			3.2		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =2A, R _G =25Ω (Note 1, 2)		3.2		ns
Rise Time		t _R			15		ns
Turn-OFF Delay Time		t _{D(OFF)}			18		ns
Fall-Time		t _F			26		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				2	A
Maximum Body-Diode Pulsed Current (Note 1)		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =2A, V _{GS} =0V,		314		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		1		μC

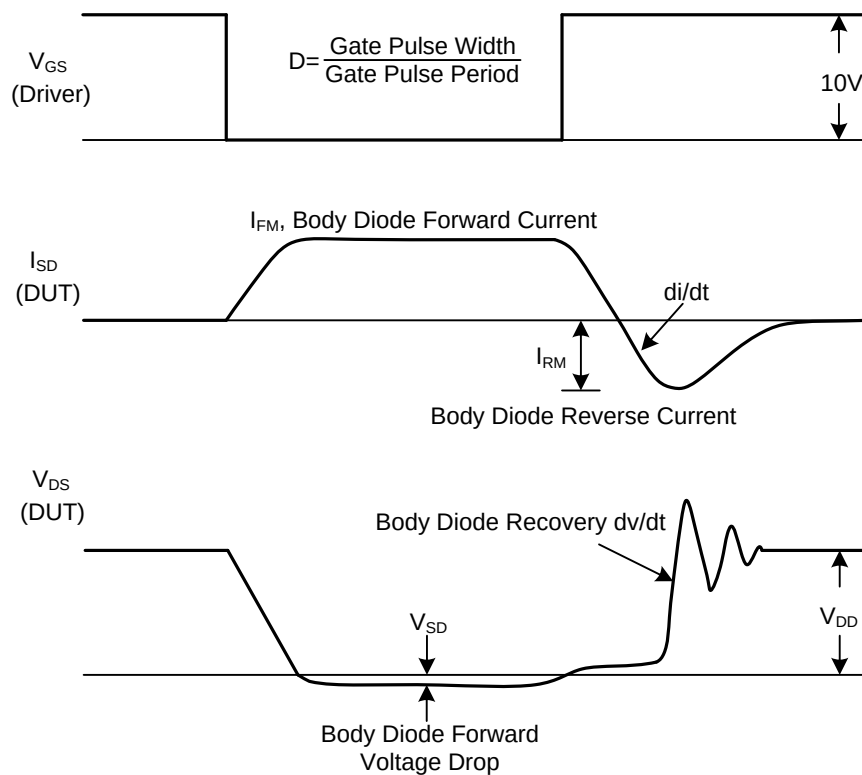
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

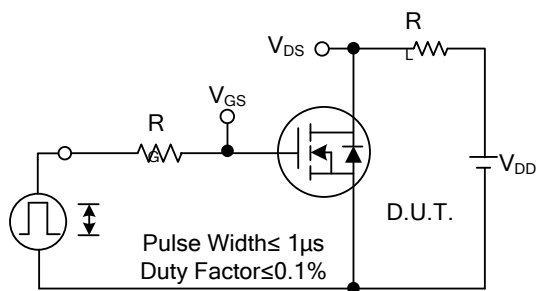


Peak Diode Recovery dv/dt Test Circuit

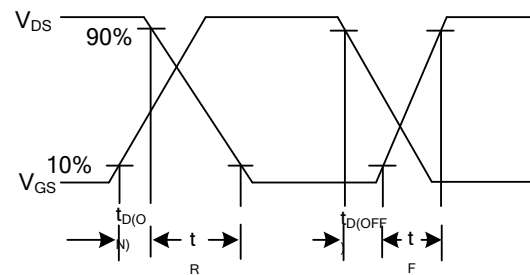


Peak Diode Recovery dv/dt Waveforms

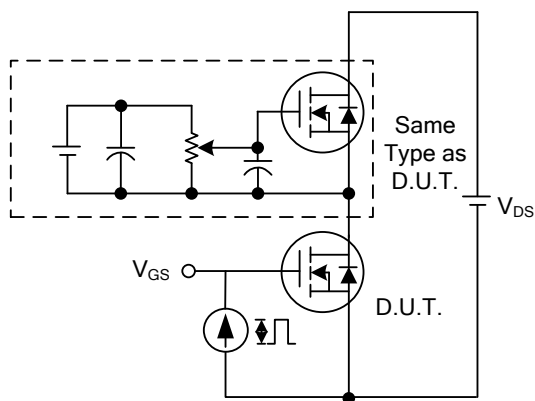
■ TEST CIRCUITS AND WAVEFORMS



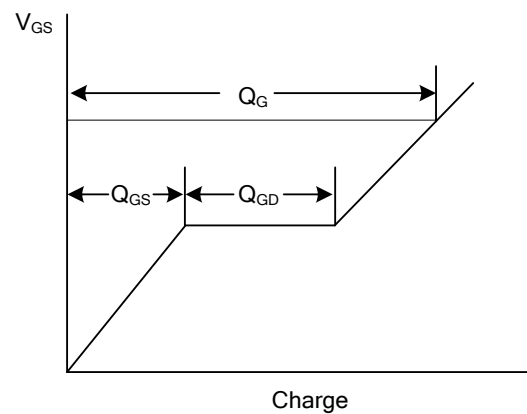
Switching Test Circuit



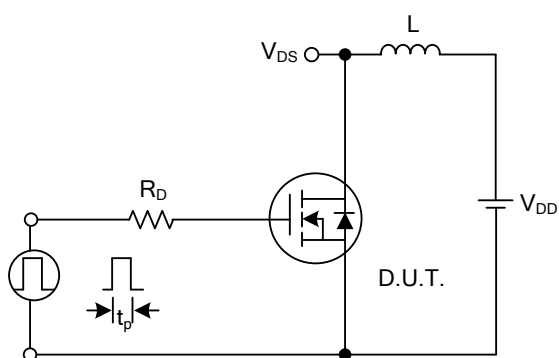
Switching Waveforms



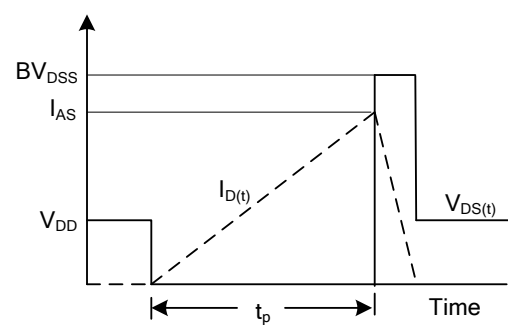
Gate Charge Test Circuit



Gate Charge Waveform

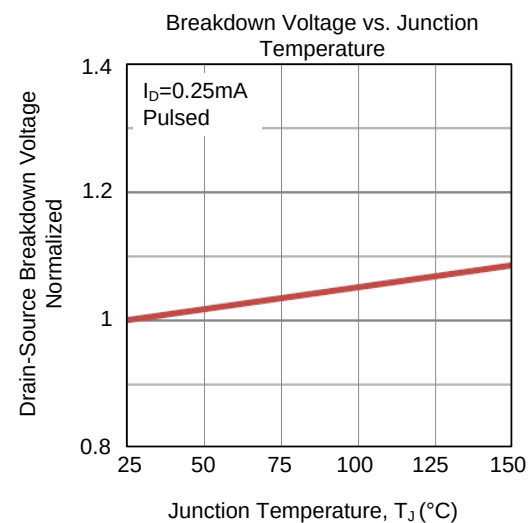
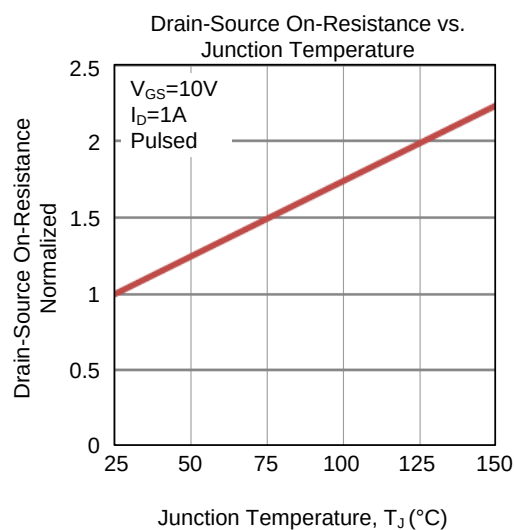
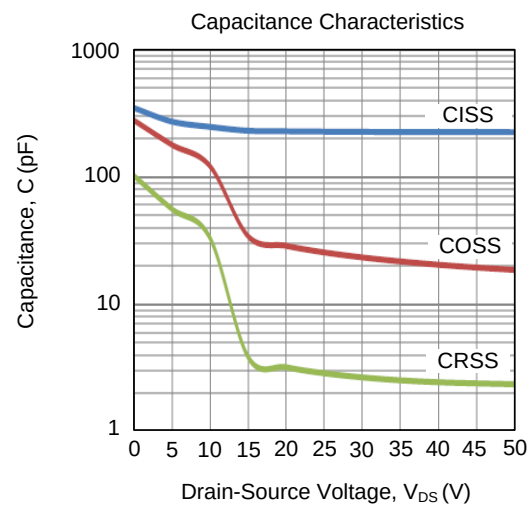
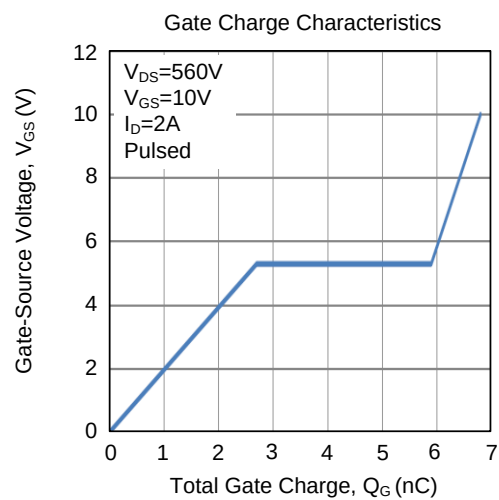
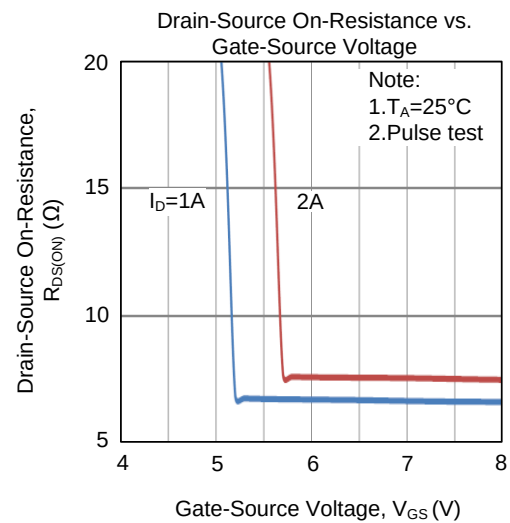
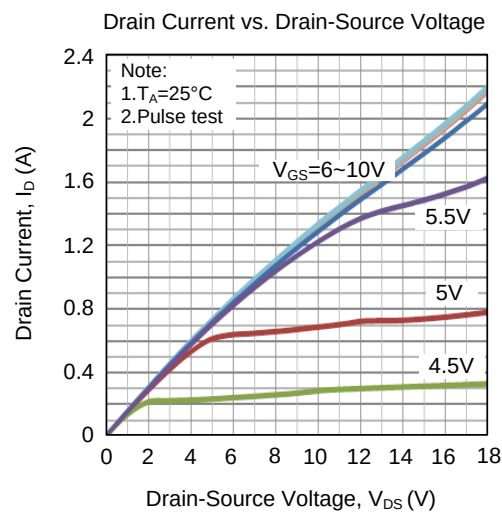


Unclamped Inductive Switching Test Circuit

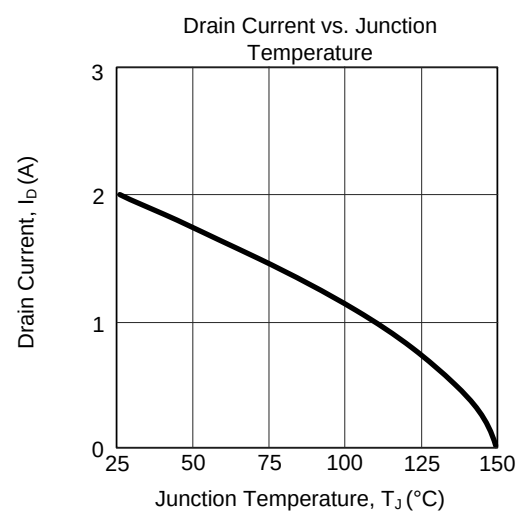
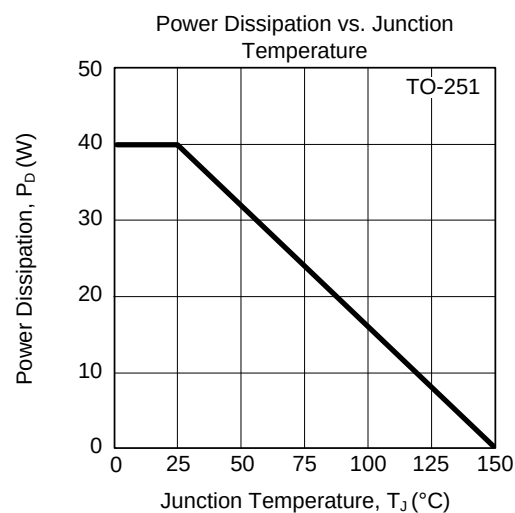
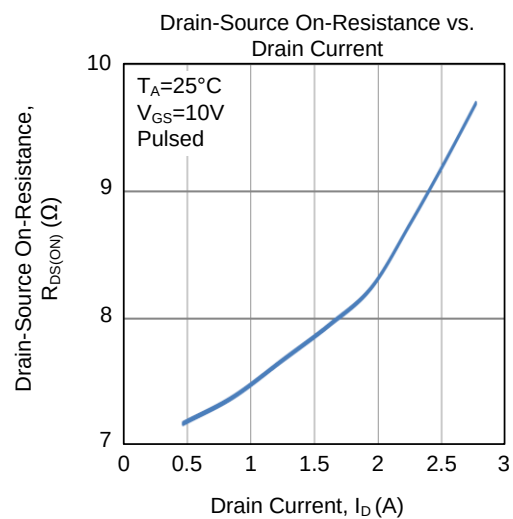
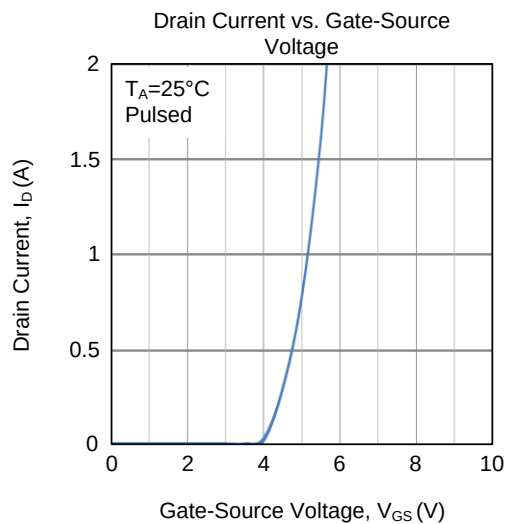
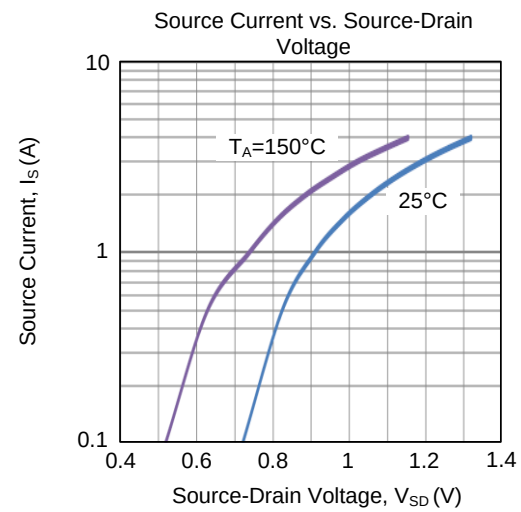
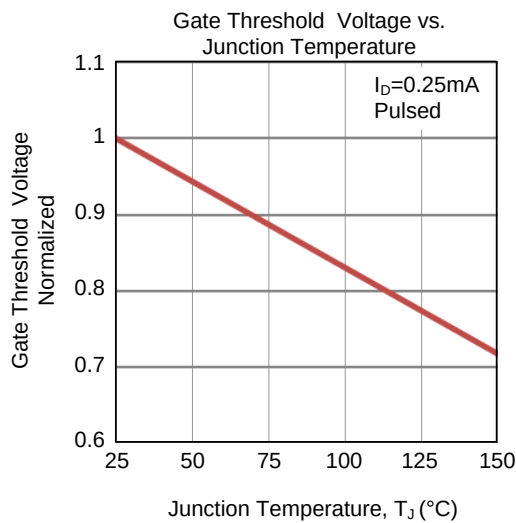


Unclamped Inductive Switching Waveforms

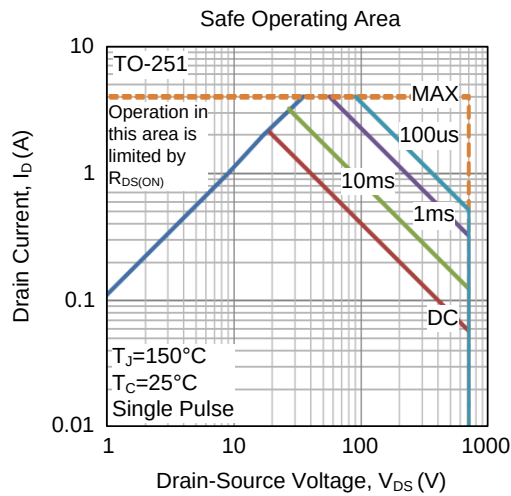
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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