

**D1NM70-Q**

Preliminary

Power MOSFET

1.0A, 700V DUAL N-CHANNEL SUPER-JUNCTION MOSFET

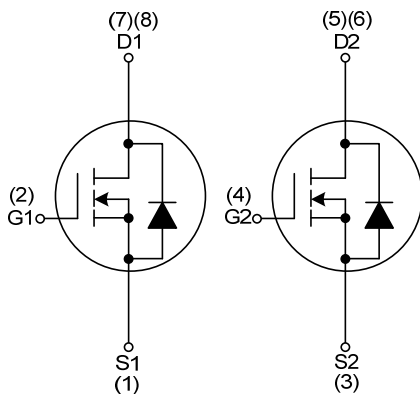
DESCRIPTION

The UTC **D1NM70-Q** is a dual Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} \leq 6.5 \Omega$ @ $V_{GS}=10V$, $I_D=0.5A$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL

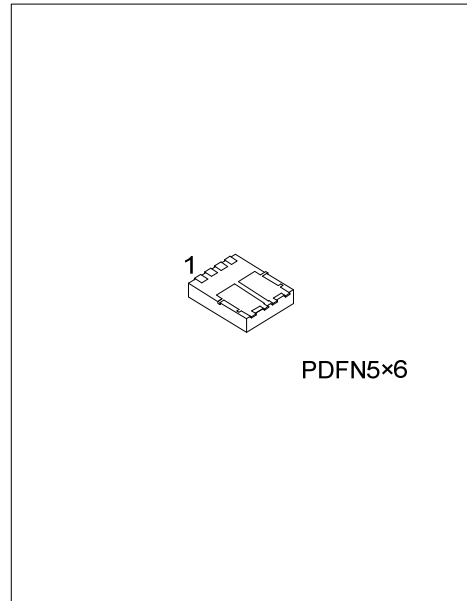


ORDERING INFORMATION

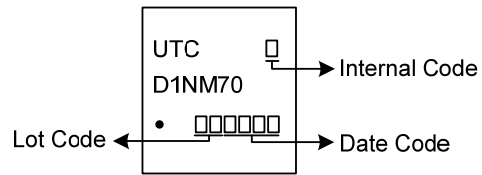
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
D1NM70L-P5060-R	D1NM70G-P5060-R	PDFN5×6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

D1NM70G-P5060-R (1) Packing Type (2) Package Type (3) Green Package		(1) R: Tape Reel (2) P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	700	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_D	1	A
Pulsed Drain Current (Note 2)	I_{DM}	2	A
Avalanche Energy (Note 3) Single Pulsed	E_{AS}	41.7	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3.9	V/ns
Power Dissipation ($T_A=25^{\circ}\text{C}$)	P_D	16	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=138\text{mH}$, $I_{AS}=0.77\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD}\leq 1.0\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	35	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	7.8	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

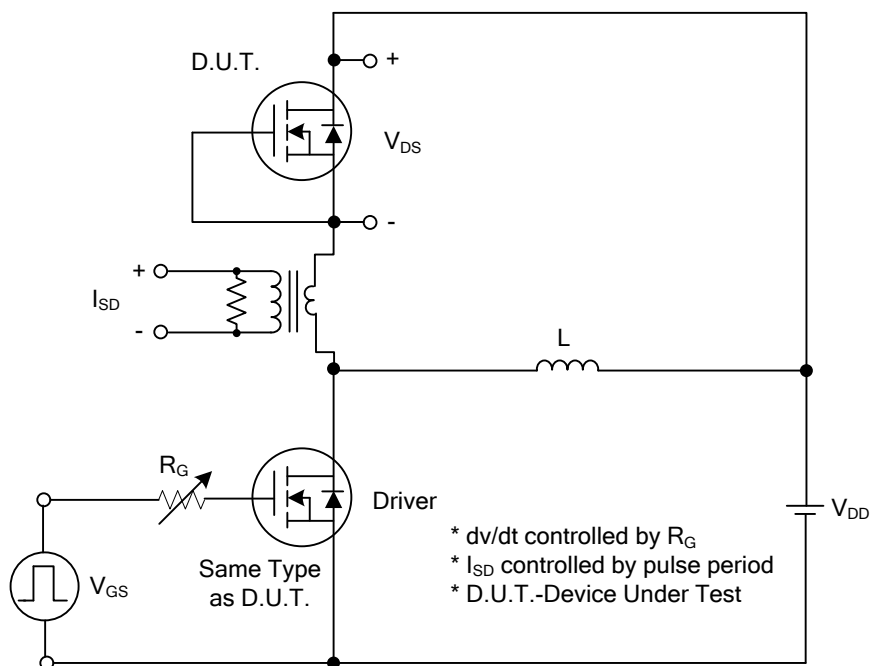
■ **ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} = 0V, I _D = 250μA	700			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} = 700V, V _{GS} = 0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} = 30V, V _{DS} = 0V			100	nA
	Reverse		V _{GS} = -30V, V _{DS} = 0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} = 10V, I _D =0.5A		5.2	6.5	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f =1MHz		90.1		pF
Output Capacitance		C _{OSS}			71.8		pF
Reverse Transfer Capacitance		C _{RSS}			9		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge		Q _G	V _{DS} =560V, V _{GS} =10V, I _D =1A, I _G =1mA (Note 1, 2)		9.1		nC
Gate-Source Charge		Q _{GS}			3.3		nC
Gate-Drain Charge		Q _{GD}			1.5		nC
Turn-On Delay Time		t _{D (ON)}	V _{DD} =100V, V _{GS} =10V, I _D =1A, R _G =25Ω (Note 1, 2)		4		ns
Turn-On Rise Time		t _R			17		ns
Turn-Off Delay Time		t _{D (OFF)}			19.6		ns
Turn-Off Fall Time		t _F			48.3		ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				1	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SD}				2	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =1.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _F =1.0A, V _{DD} =100V		198		ns
Reverse Recovery Charge		Q _{rr}	di/dt = 100A/μs		1.3		μC

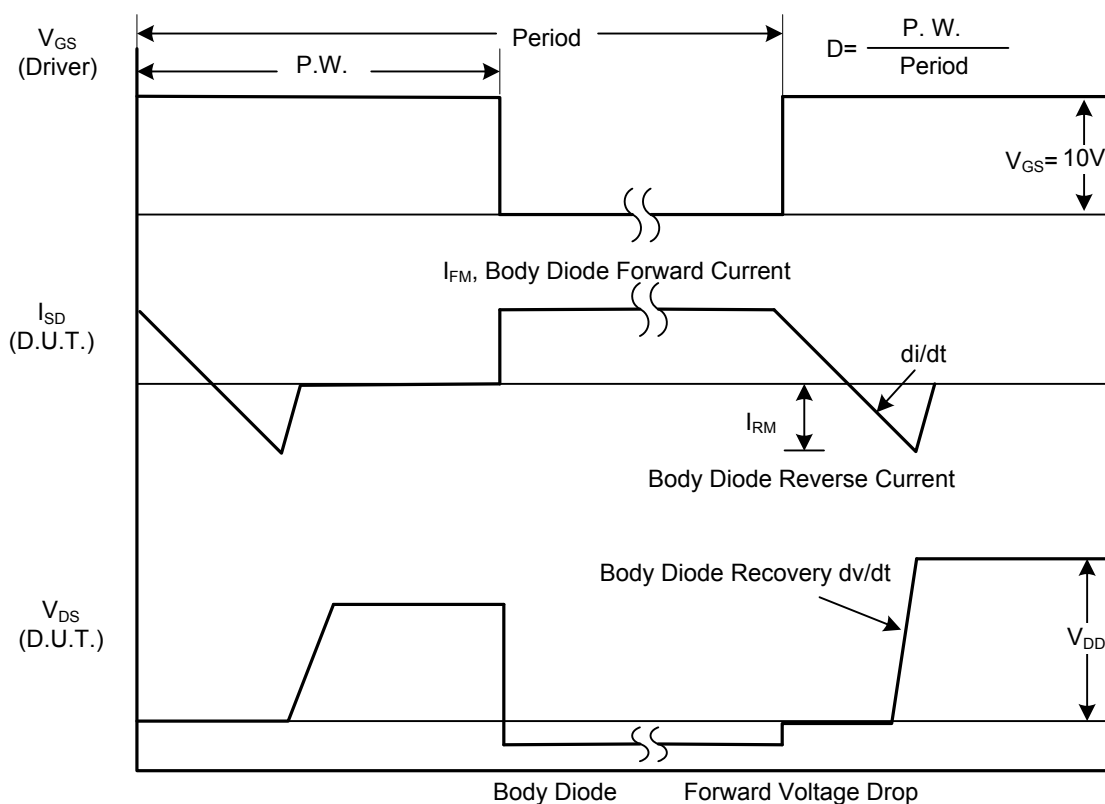
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

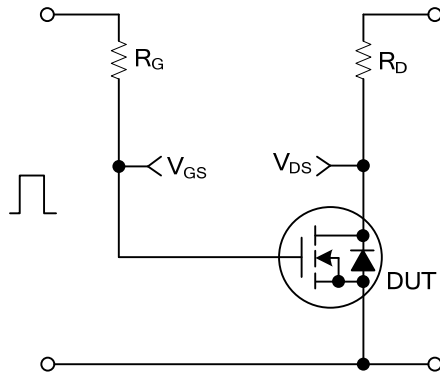


Peak Diode Recovery dv/dt Test Circuit

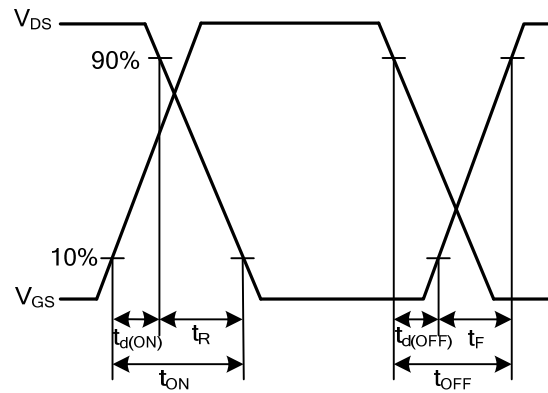


Peak Diode Recovery dv/dt Waveforms

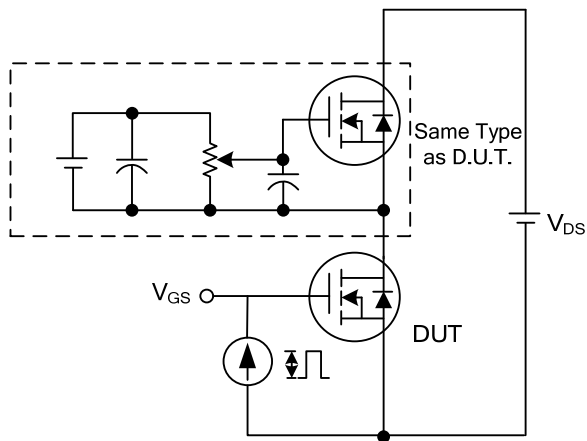
■ TEST CIRCUITS AND WAVEFORMS



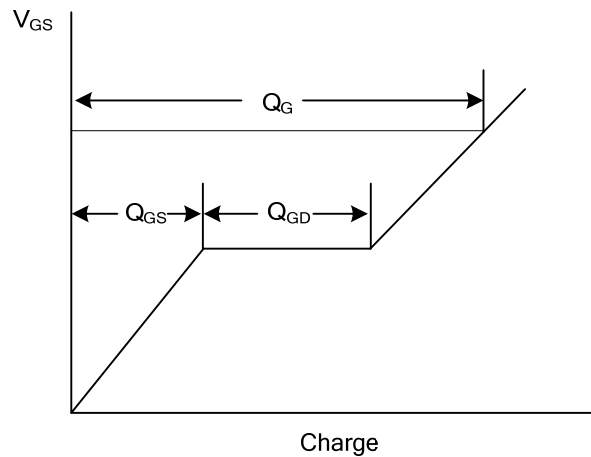
Switching Test Circuit



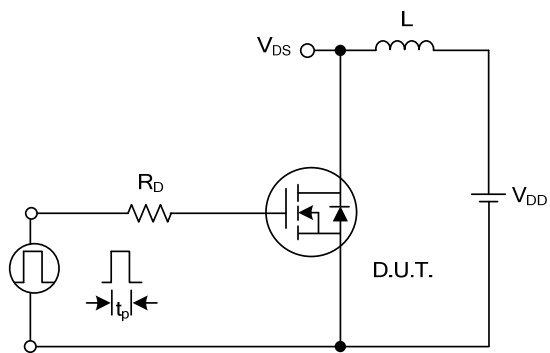
Switching Waveforms



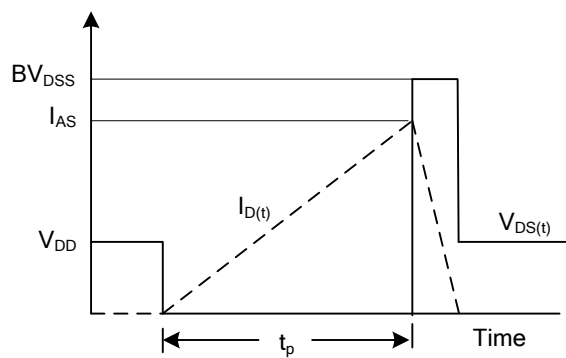
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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