

**F5N60-TD1**

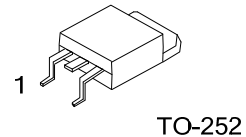
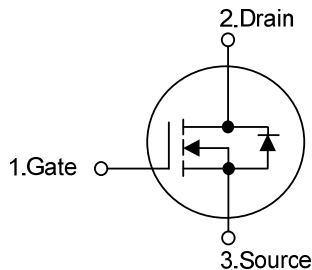
Preliminary

Power MOSFET**5.0A, 600V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **F5N60-TD1** is a N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode, is designed high voltage, high speed power switching applications such, is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} \leq 2.5 \Omega$ @ $V_{GS}=10V$, $I_D=2.5A$
- * Fast body diode MOSFET technology
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

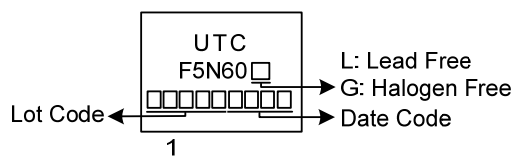
SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F5N60L-TN3-R	F5N60G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

F5N60G-TN3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	86	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.8	V/ns
Power Dissipation		P_D	54	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=30\text{mH}$, $I_{AS}=2.4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.31 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

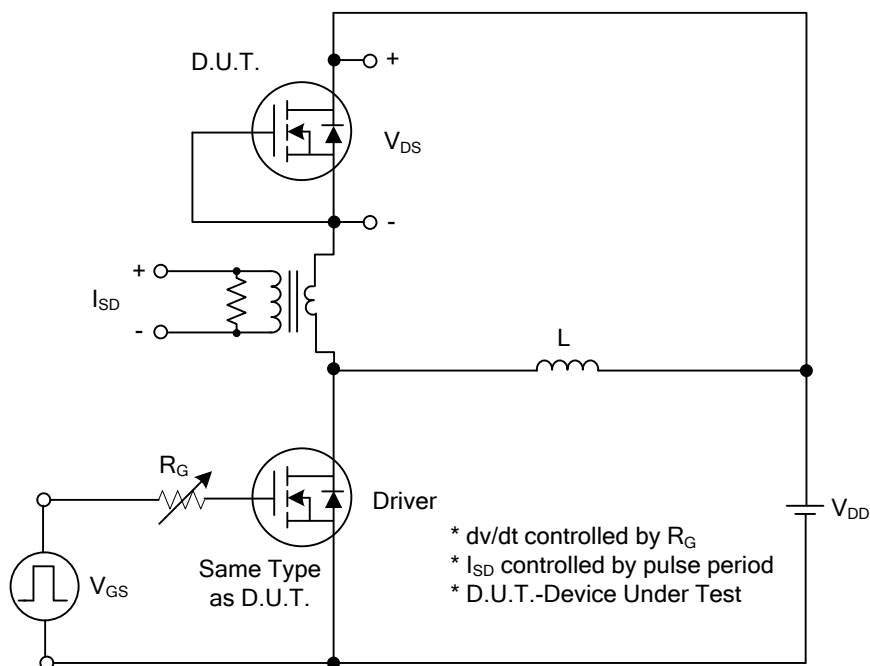
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =30V, V _{DS} =0V			100	nA
		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Drain to Source On-state Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =2.5A			2.5	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		635		pF
Output Capacitance	C _{OSS}			62.5		pF
Reverse Transfer Capacitance	C _{RSS}			3.5		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =480V, V _{GS} =10V, I _D =5A, I _G =1mA (Note 1, 2)		20		nC
Gate Source Charge	Q _{GS}			6.2		nC
Gate Drain Charge	Q _{GD}			3.2		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =5A, R _G =25Ω (Note 1, 2)		8		ns
Turn-ON Rise Time	t _R			17		ns
Turn-OFF Delay Time	t _{D(OFF)}			41		ns
Turn-OFF Fall-Time	t _F			27		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				5	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				10	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =5A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)	t _{rr}	I _S =5A, V _{GS} =0V, dI/dt=100A/μs		112		ns
Reverse Recovery Charge	Q _{rr}			540		nC

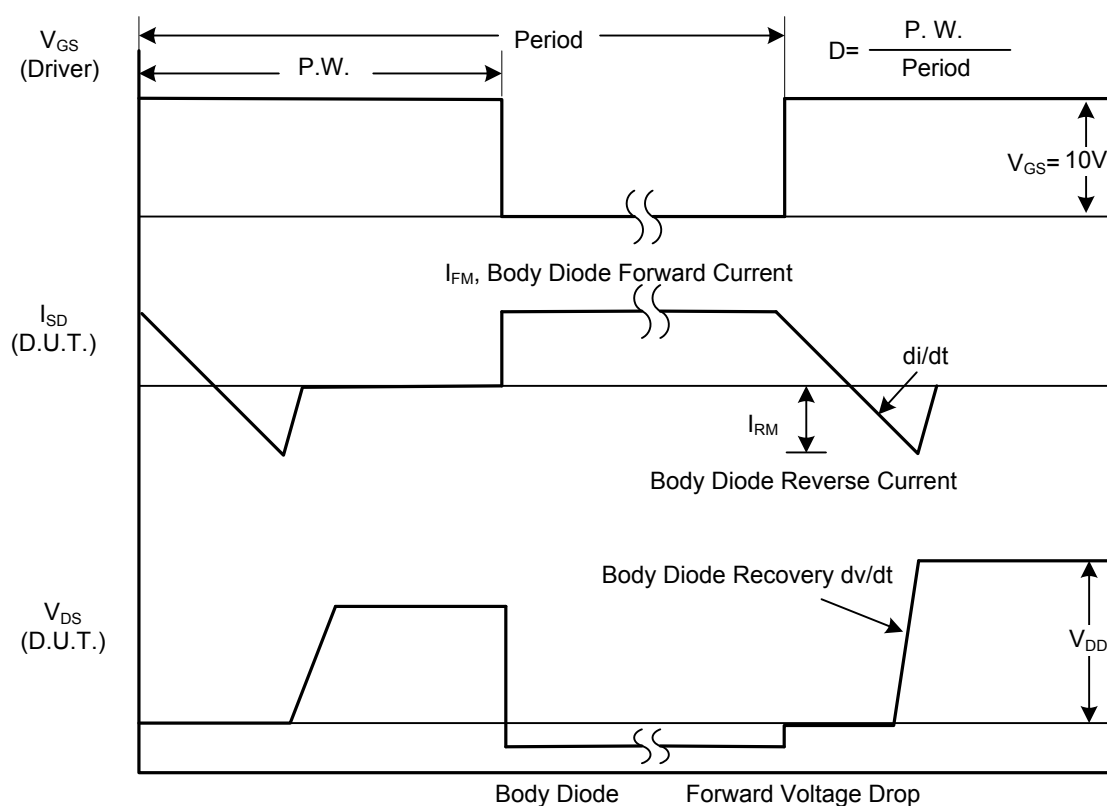
Notes: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

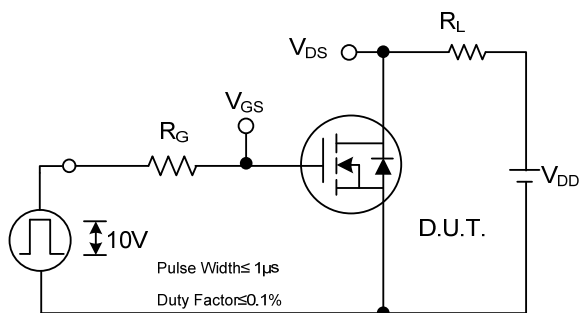


Peak Diode Recovery dv/dt Test Circuit

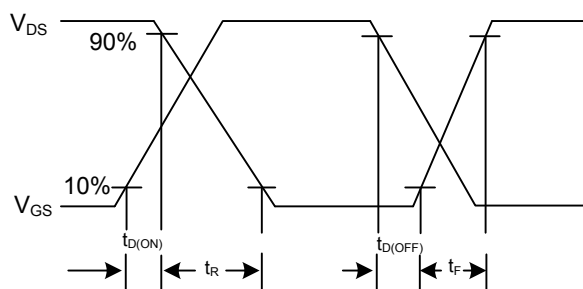


Peak Diode Recovery dv/dt Waveforms

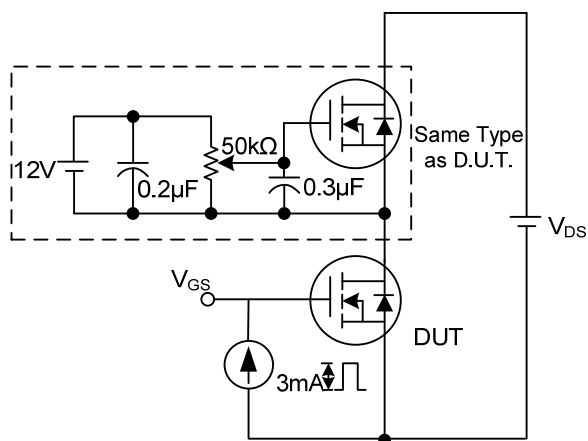
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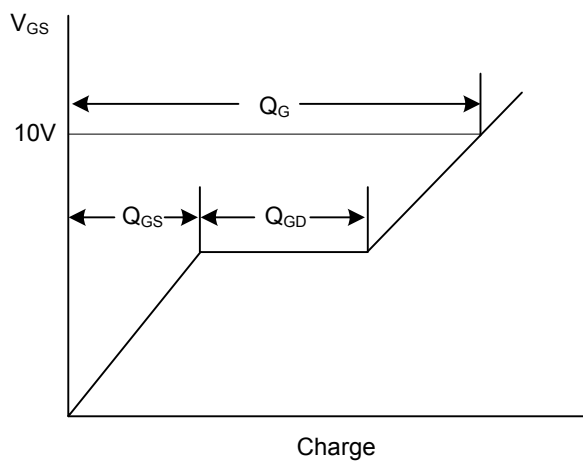
Switching Test Circuit



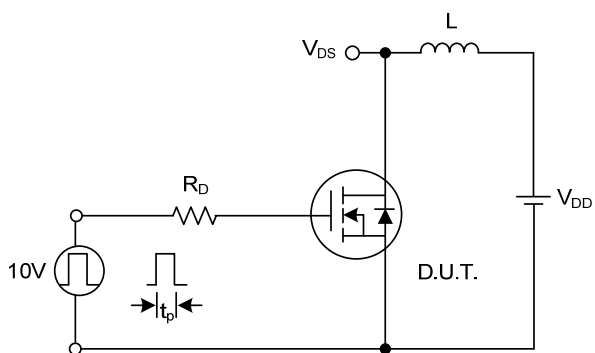
Switching Waveforms



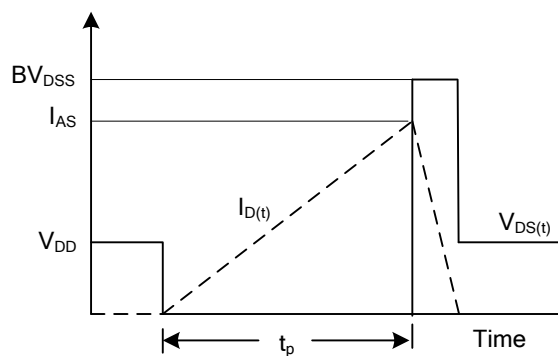
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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