



U74ACT04

CMOS IC

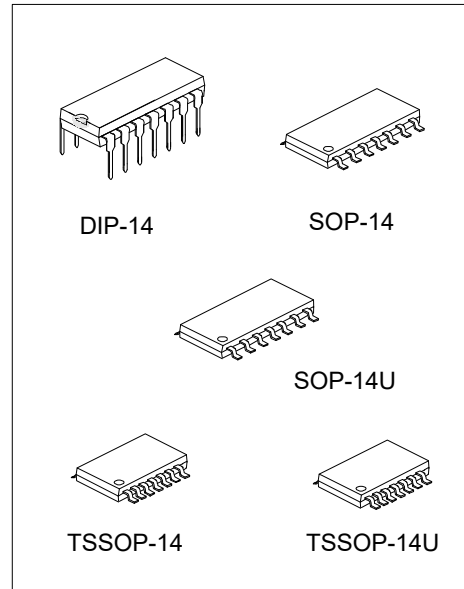
HEX INVERTERS

DESCRIPTION

The UTC **U74ACT04** contains six independent inverters and each of them performs the Boolean function $Y=\bar{A}$.

FEATURES

* Inputs are TTL Voltage Compatible



ORDERING INFORMATION

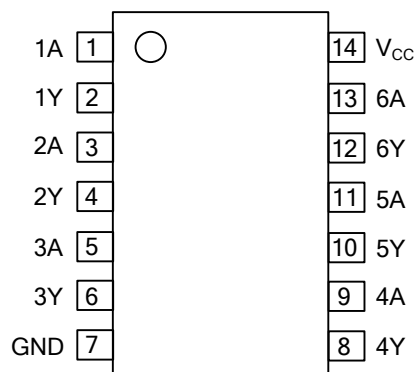
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74ACT04L-D14-T	U74ACT04G-D14-T	DIP-14	Tube
U74ACT04L-S14-R	U74ACT04G-S14-R	SOP-14	Tape Reel
U74ACT04L-UEA-R	U74ACT04G-UEA-R	SOP-14U	Tape Reel
U74ACT04L-P14-R	U74ACT04G-P14-R	TSSOP-14	Tape Reel
U74ACT04L-UEB-R	U74ACT04G-UEB-R	TSSOP-14U	Tape Reel

U74ACT04G-D14-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) D14: DIP-14, S14: SOP-14, UEA: SOP-14 P14: TSSOP-14, UEB: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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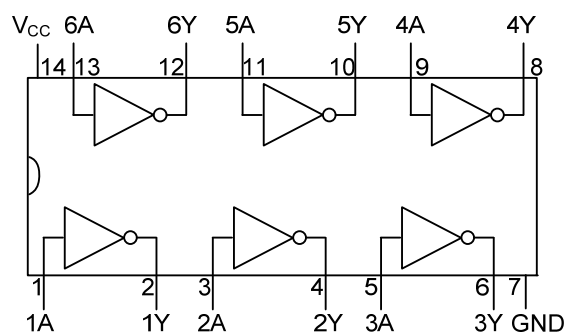
MARKING

DIP-14	SOP-14 / TSSOP-14
14 13 12 11 10 9 8 UTC □□□□ U74ACT04 □ □□ 1 2 3 4 5 6 7 → Date Code L: Lead Free G: Halogen Free → Lot Code	14 13 12 11 10 9 8 UTC □□□□ U74ACT04 □ □□ 1 2 3 4 5 6 7 → Date Code L: Lead Free G: Halogen Free → Lot Code

PIN CONFIGURATION



FUNCTIONAL DIAGRAM

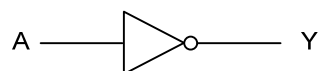


FUNCTION TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

Note: H=High level; L=Low Level

LOGIC DIAGRAM



■ **ABSOLUTE MAXIMUM RATING** (T_A=25°C, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7.0	V
Input Voltage	V _{IN}	-0.5 ~ V _{CC} +0.5	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	I _{IK}	±20	mA
Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	I _{OK}	±20	mA
Output Current (V _{OUT} =0 to V _{CC})	I _{OUT}	±50	mA
V _{CC} or GND Current	I _{CC}	±200	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS** (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	4.5 ~ 5.5	V
Input Voltage	V _{IN}	0 ~ V _{CC}	V
Output Voltage	V _{OUT}	0 ~ V _{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	8	ns/V
Operating Temperature	T _A	-40 ~ +125	°C

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-14	90	°C/W
	SOP-14	95	°C/W
	SOP-14U		
	TSSOP-14	120	°C/W
	TSSOP-14U		

■ **ELECTRICAL CHARACTERISTICS** (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High Level Input Voltage	V _{IH}	V _{CC} =4.5~5.5V	2			V
Low Level Input Voltage	V _{IL}	V _{CC} =4.5~5.5V			0.8	V
High-Level Output Voltage	V _{OH}	V _{CC} =4.5V	I _{OH} =-24mA	3.86		V
			I _{OH} =-50μA	4.4	4.49	V
		V _{CC} =5.5V	I _{OH} =-24mA	4.86		V
			I _{OH} =-50μA	5.4	5.49	V
Low-Level Output Voltage	V _{OL}	V _{CC} =4.5V	I _{OL} =24mA		0.36	V
			I _{OL} =50μA	0.001	0.1	V
		V _{CC} =5.5V	I _{OL} =24mA		0.36	V
			I _{OL} =50μA	0.001	0.1	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND			±0.1	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0			2	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _Q	V _{CC} =5.5V, One input at 3.4V, Other inputs at GND or V _{CC}		0.6		mA
Input Capacitance	C _{IN}	V _{CC} =5V, V _{IN} =V _{CC} or GND		4.5		pF

■ **SWITCHING CHARACTERISTICS** (Input t_R , $t_F = 2.5\text{ns}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH}	$V_{CC} = 5 \pm 0.5\text{V}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$	1	6	8.5	ns
	t_{PHL}		1	5.5	8	ns

■ **OPERATING CHARACTERISTICS** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC} = 5\text{V}$, $C_L = 50\text{pF}$, $f = 1\text{MHz}$		45		pF

Notes: 1. C_{PD} is used to determine the dynamic power consumption, per inverter.

2. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

■ TEST CIRCUITS AND WAVEFORMS

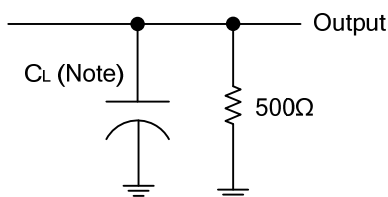


Figure 1. Load circuitry for switching times

Note: C_L includes probe and jig capacitance.

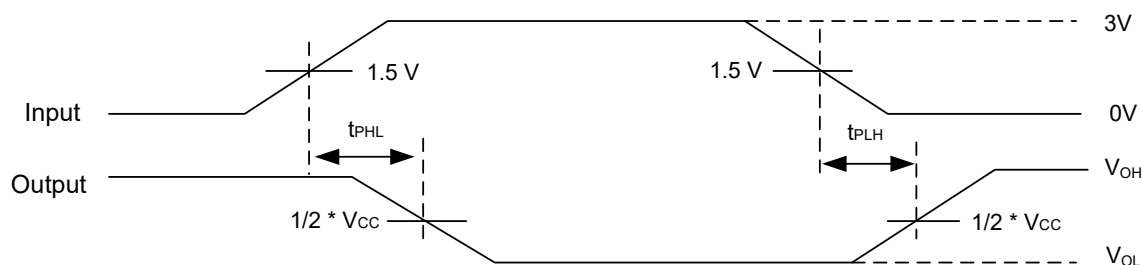


Figure 2. Propagation delay from Input (A) to Output (Y)

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