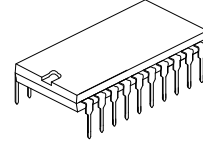


**U74AHC541****CMOS IC****OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS****DESCRIPTION**

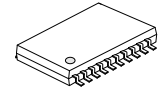
The **U74AHC541** is a octal buffers/drivers with 3-state outputs and 8 channels.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

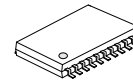
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



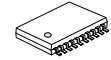
DIP-20



SOP-20



SSOP-20



TSSOP-20U

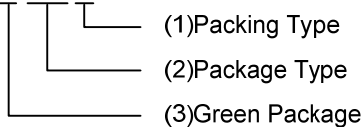
FEATURES

- * Operate from 2V to 5.5V
- * Balanced propagation delays
- * Inputs accepts voltages higher than V_{CC}

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC541L-D20-T	U74AHC541G-D20-T	DIP-20	Tube
U74AHC541L-S20-R	U74AHC541G-S20-R	SOP-20	Tape Reel
U74AHC541L-R20-R	U74AHC541G-R20-R	SSOP-20	Tape Reel
U74AHC541L-ULA-R	U74AHC541G-ULA-R	TSSOP-20U	Tape Reel

U74AHC541G-D20-T



(1) T: Tube, R: Tape Reel

(2) D20: DIP-20, S20: SOP-20, R20: SSOP-20

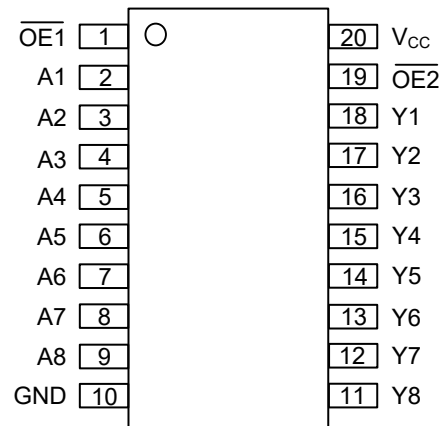
ULA: TSSOP-20U

(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

DIP-20	SOP-20 / SSOP-20 / TSSOP-20U
→ Date Code → L: Lead Free → G: Halogen Free → Lot Code	→ Date Code → L: Lead Free → G: Halogen Free → Lot Code

PIN CONFIGURATION

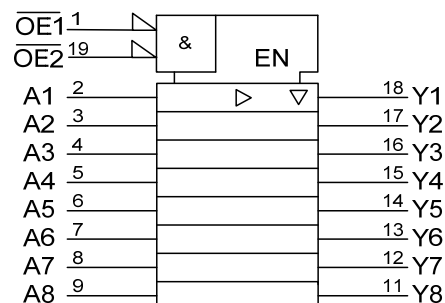


FUNCTION TABLE

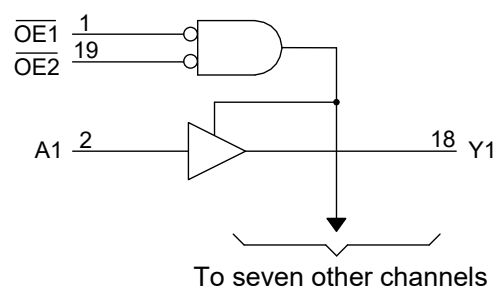
INPUTS $\overline{OE1}$	INPUTS $\overline{OE2}$	INPUTS(A)	OUTPUT(Y)
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level ; L = Low voltage level ; X = Don't care

LOGIC SYMBOL



LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
Input Voltage	V_{IN}	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	-0.5 ~ 7	V
Output Voltage	V_{OUT}		-0.5 ~ $V_{CC} + 0.5$	V
Continuous current through V_{CC} or GND	I_{CC}		±75	mA
Continuous Output Current	I_{OUT}	$V_{OUT} = 0 \sim V_{CC}$	±25	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0$	-20	mA
Output Clamp Current	I_{OK}	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	±20	mA
Storage Temperature	T_{STG}		-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	$T_A = 25^\circ\text{C}$			$T_A = -40 \sim +125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage	V_{CC}		2		5.5	2		5.5	V
High-Level Input Voltage	V_{IH}	$V_{CC} = 2\text{V}$	1.5			1.5			V
		$V_{CC} = 3\text{V}$	2.1			2.1			V
		$V_{CC} = 5.5\text{V}$	3.85			3.85			V
Low-Level Input Voltage	V_{IL}	$V_{CC} = 2\text{V}$			0.5			0.5	V
		$V_{CC} = 3\text{V}$			0.9			0.9	V
		$V_{CC} = 5.5\text{V}$			1.65			1.65	V
Input Voltage	V_{IN}		0		5.5	0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t / \Delta v$	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			100			100	ns/V
		$V_{CC} = 5\text{V} \pm 0.5\text{V}$			20			20	
Operating Temperature	T_A		-40		+125	-40		+125	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	θ_{JA}	90	°C/W
	SOP-20		115	°C/W
	SSOP-20		130	°C/W
	TSSOP-20U		135	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	V _{OH}	V _{CC} =2V, I _{OH} =-50μA	1.9			1.9			V
		V _{CC} =3V, I _{OH} =-50μA	2.9			2.9			V
		V _{CC} =4.5V, I _{OH} =-50μA	4.4			4.4			V
		V _{CC} =3V, I _{OH} =-4mA	2.58			2.40			V
		V _{CC} =4.5V, I _{OH} =-8mA	3.94			3.70			V
Low-Level Output Voltage	V _{OL}	V _{CC} =2V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =3V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =3V, I _{OL} =4mA			0.36			0.55	V
		V _{CC} =4.5V, I _{OL} =8mA			0.36			0.55	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0~5.5V, V _{IN} =5.5V or GND			±0.1			±2.0	μA
Output Off-state Current	I _{oz}	V _{CC} =5.5V, V _{IN} ($\overline{\text{OE}}$)=V _{IL} or V _{IH} , V _{OUT} =V _{CC} or GND			±0.25			±10	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			4			80	μA

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (A) to output (Y)	t _{PLH} / t _{PHL}	V _{CC} =3.3V±0.3V		5.0	8.0	1.0		9.0	ns
		V _{CC} =5V±0.5V		7.5	11.5	1.0		13.5	ns
Propagation delay from input ($\overline{\text{OE}}$) to output (Y)	t _{PZL} / t _{PZH}	V _{CC} =3.3V±0.3V		6.0	11.5	1.0		13.5	ns
		V _{CC} =5V±0.5V		8.0	14	1.0		17.5	ns
Output Disable Time From ($\overline{\text{OE}}$) to output (Y)	t _{PLZ} / t _{PHZ}	V _{CC} =3.3V±0.3V		7.0	11	1.0		14	ns
		V _{CC} =5V±0.5V		9.0	15.5	1.0		19.5	ns
Output Skew Time	t _{SK(O)}	V _{CC} =3.3V±0.3V			1.5				ns
		V _{CC} =5V±0.5V			1.0				ns

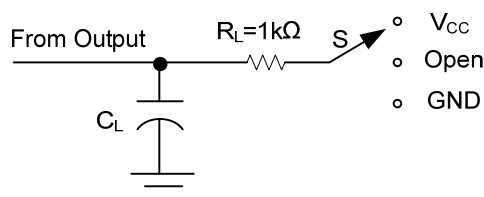
■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}				0.8	V
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}				-0.8	V
Quiet output, minimum dynamic V _{OH}	V _{OH(V)}		4.7			V
High-level dynamic input voltage	V _{IH(D)}		3.5			V
Low-level dynamic input voltage	V _{IL(D)}				1.5	V

■ OPERATING CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	$V_{CC}=5.5\text{V}$, $V_{IN}=V_{CC}$ or GND		2	10	pF
Output Capacitance	C_{OUT}	$V_{CC}=5.5\text{V}$, $V_{OUT}=V_{CC}$ or GND		4		pF
Power Dissipation Capacitance per flip-flop	C_{PD}	$V_{CC}=5\text{V}$, $f=1\text{MHz}$, No load.		12		pF

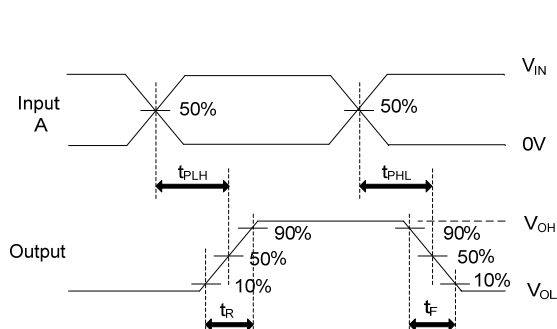
■ TEST CIRCUIT AND WAVEFORMS



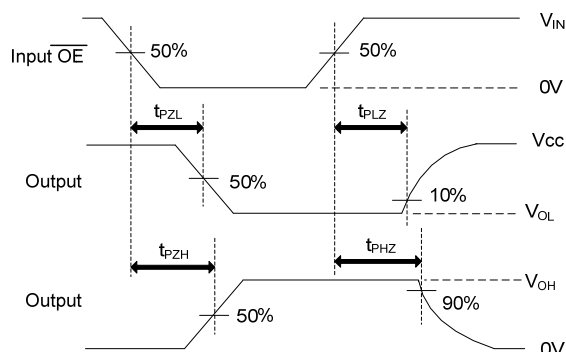
TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

Parameter		R_L	C_L
t_{en}	t_{PZH}	1KΩ	15 pF or 50 pF
	t_{PZL}		
t_{dis}	t_{PHZ}	1KΩ	15 pF or 50 pF
	t_{PLZ}		
t_{PD} or t_t			15 pF or 50 pF



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 1\text{MHz}$, $Z_0 = 50\Omega$,

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