



UT3N06-L

Power MOSFET

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

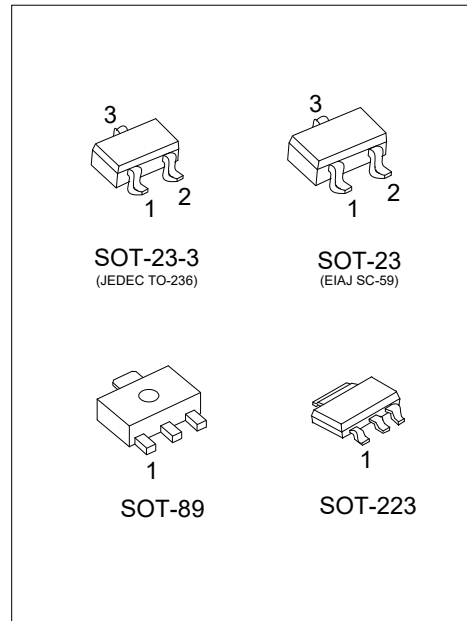
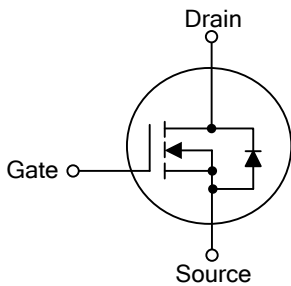
DESCRIPTION

The UTC **UT3N06-L** is an N-channel power MOSFET providing very low on-resistance. It has high efficiency and perfect cost-effectiveness. It can be generally applied in the commercial and industrial fields.

FEATURES

* Simple drive requirement

SYMBOL



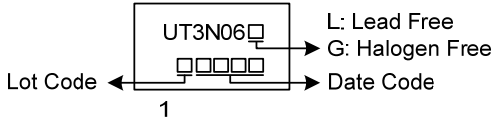
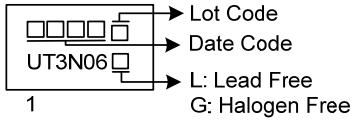
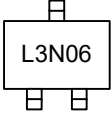
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT3N06L-AA3-R	UT3N06G-AA3-R	SOT-223	G	D	S	Tape Reel
UT3N06L-AB3-R	UT3N06G-AB3-R	SOT-89	G	D	S	Tape Reel
UT3N06L-AE2-R	UT3N06G-AE2-R	SOT-23-3	G	S	D	Tape Reel
UT3N06L-AE3-R	UT3N06G-AE3-R	SOT-23	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

<p>UT3N06G-AA3-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) AA3: SOT-223, AB3: SOT-89, AE2: SOT-23-3, AE3: SOT-23 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

SOT-223	SOT-89
 <p>Diagram of SOT-223 marking: A rectangular package with 'UT3N06' at the top, '1' at the bottom, and 'Lot Code' on the left. Arrows point from the right side to 'L: Lead Free', 'G: Halogen Free', and 'Date Code'.</p>	 <p>Diagram of SOT-89 marking: A package with 'UT3N06' and '1' on the front. Arrows point from the top to 'Lot Code' and 'Date Code', and from the right to 'L: Lead Free' and 'G: Halogen Free'.</p>
SOT-23-3 / SOT-23	-
 <p>Diagram of SOT-23-3 / SOT-23 marking: A package with 'L3N06' on the front.</p>	-

■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	3	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	6	A
Power Dissipation	SOT-223	P_D	1.25	W
	SOT-23-3		0.3	W
	SOT-23/SOT-89		0.5	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient	SOT-223	θ_{JA}	100	$^\circ\text{C/W}$
	SOT-23-3		416	$^\circ\text{C/W}$
	SOT-23		250	$^\circ\text{C/W}$
	SOT-89		125	$^\circ\text{C/W}$

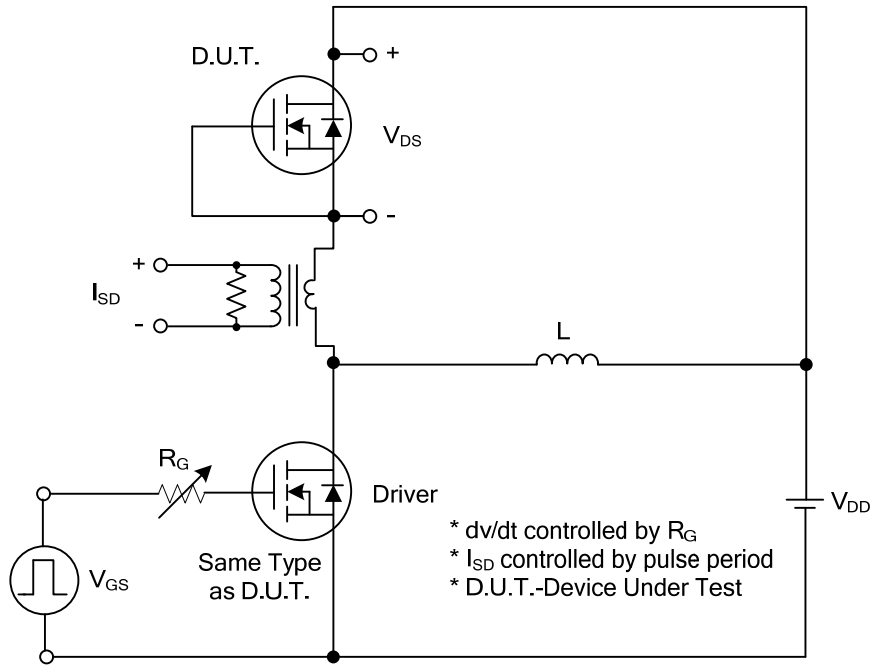
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

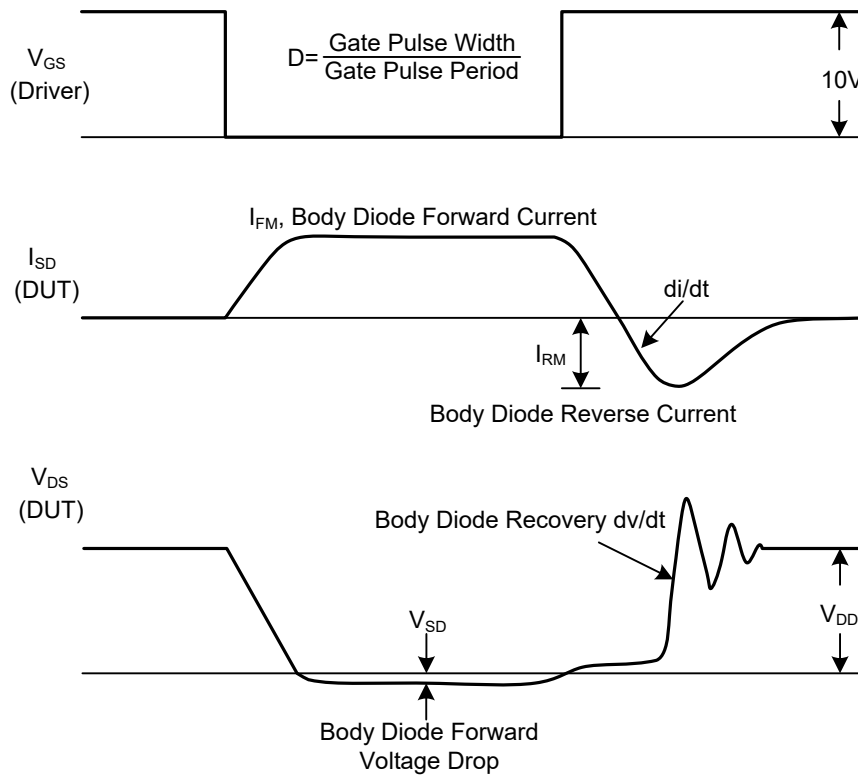
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	60			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V			1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	0.5		1.5	V
Drain to Source On-state Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 3.0A			110	mΩ
		V _{GS} = 4.5V, I _D = 2.0A			150	mΩ
		V _{GS} = 3.3V, I _D = 1.0A			250	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz		170		pF
Output Capacitance	C _{OSS}			30		pF
Reverse Transfer Capacitance	C _{RSS}			20		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note)	Q _G	V _{DS} = 48V, V _{GS} = 10V, I _D = 3.0A I _G = 1mA (Note 1, 2)		12		nC
Gate Source Charge	Q _{GS}			2		nC
Gate Drain Charge	Q _{GD}			1.8		nC
Turn-ON Delay Time (Note)	t _{D(ON)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 0.3A, R _G = 3Ω (Note 1, 2)		5		ns
Turn-ON Rise Time	t _R			14		ns
Turn-OFF Delay Time	t _{D(OFF)}			13		ns
Turn-OFF Fall-Time	t _F			8		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				3	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				6	A
Drain-Source Diode Forward Voltage (Note)	V _{SD}	I _S = 3A, V _{GS} = 0V			1.4	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

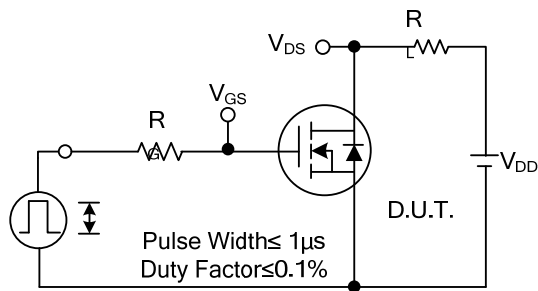


Peak Diode Recovery dv/dt Test Circuit

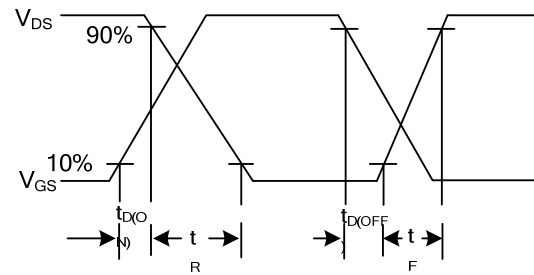


Peak Diode Recovery dv/dt Waveforms

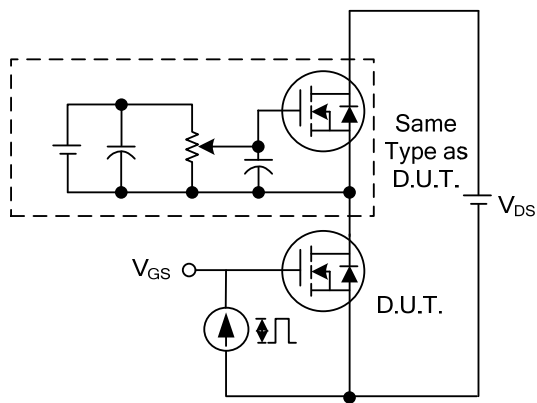
TEST CIRCUITS AND WAVEFORMS



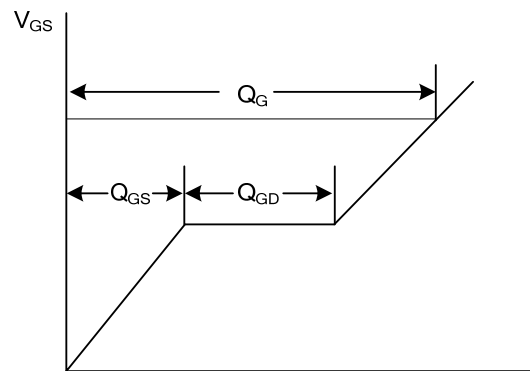
Switching Test Circuit



Switching Waveforms

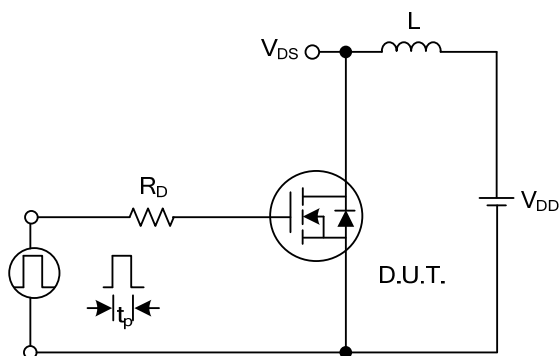


Gate Charge Test Circuit

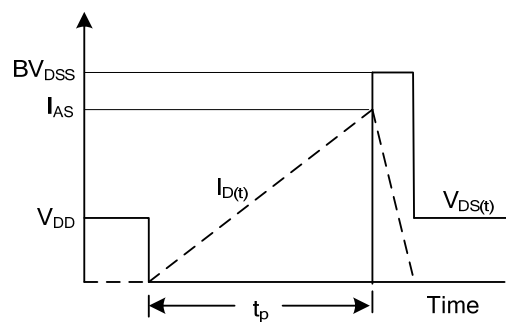


Charge

Gate Charge Waveform

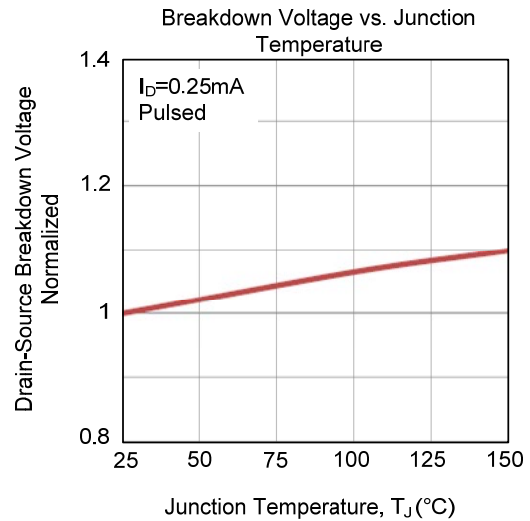
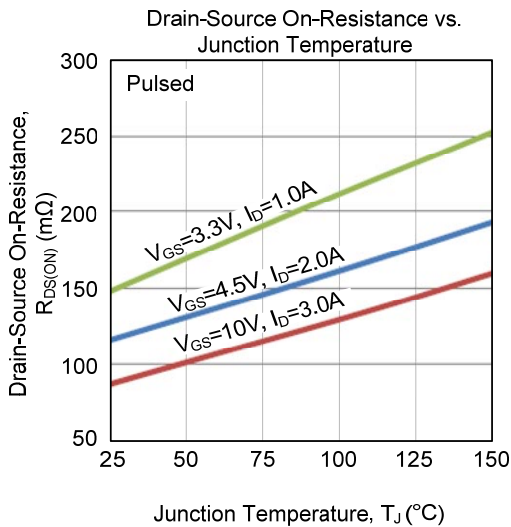
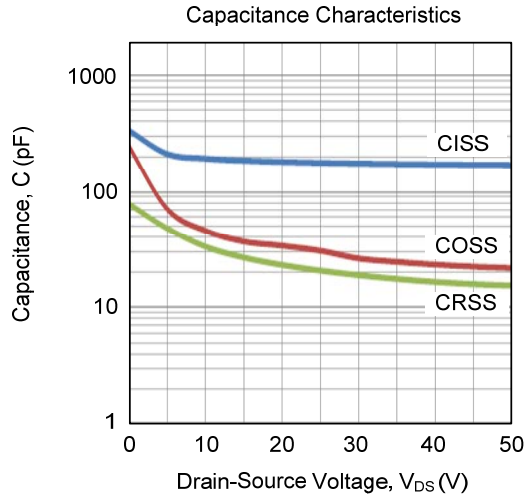
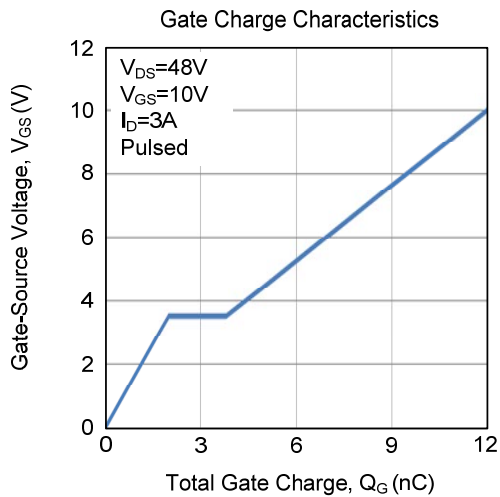
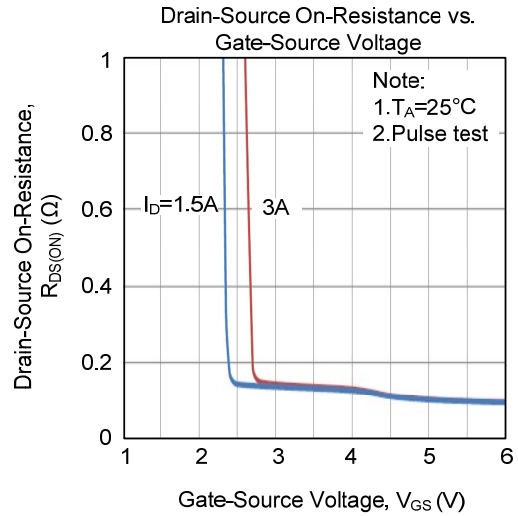
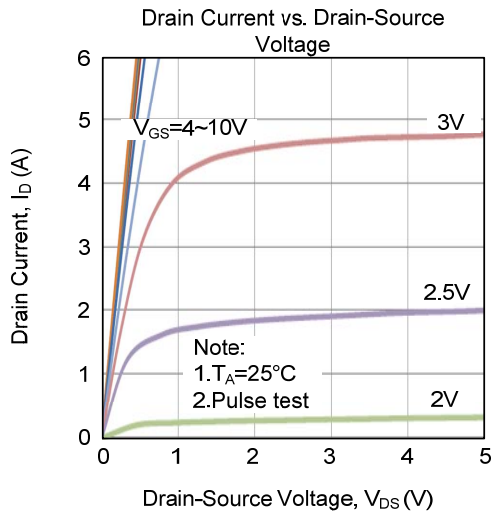


Unclamped Inductive Switching Test Circuit

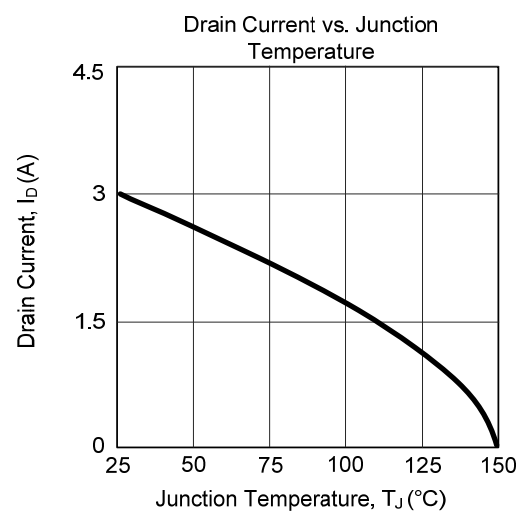
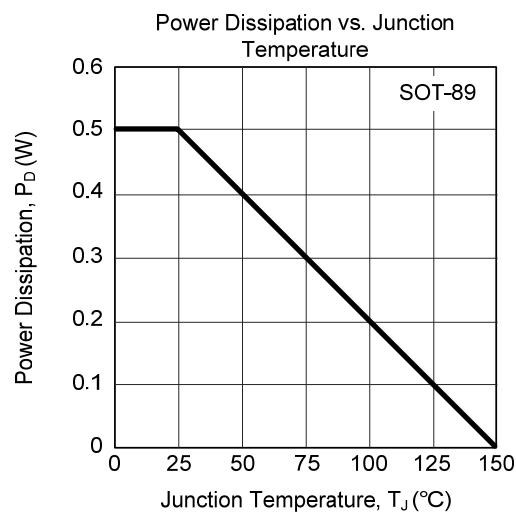
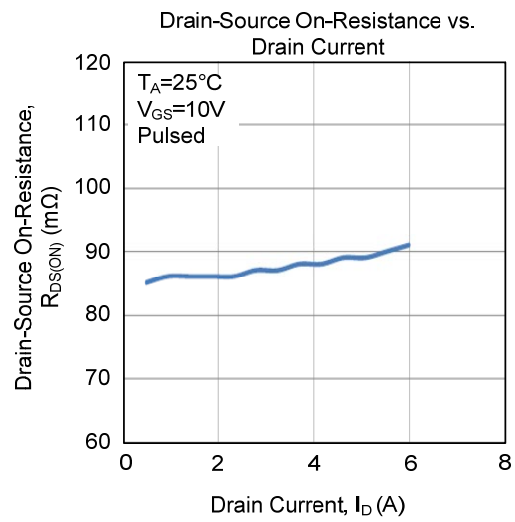
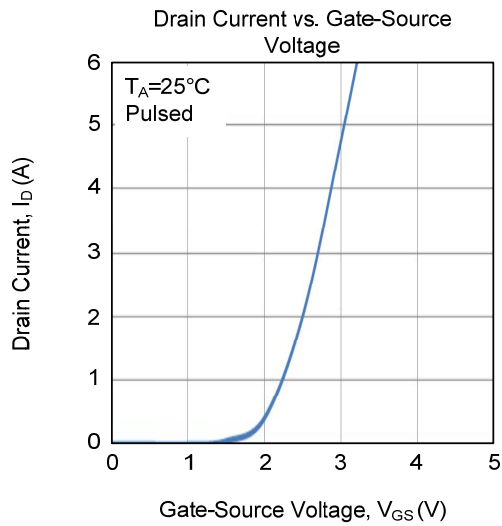
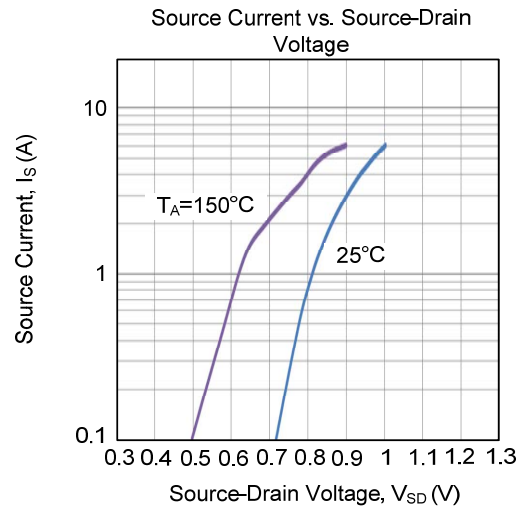
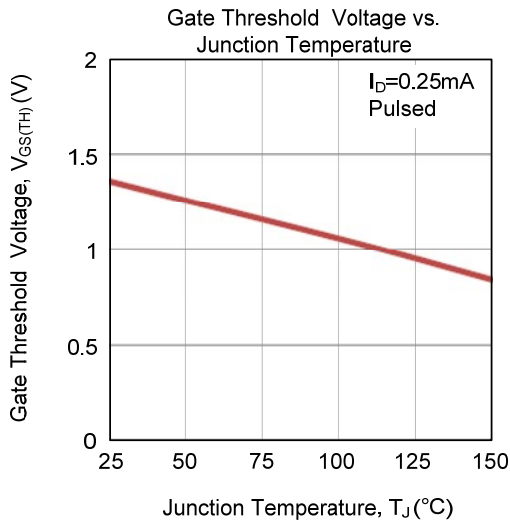


Unclamped Inductive Switching Waveforms

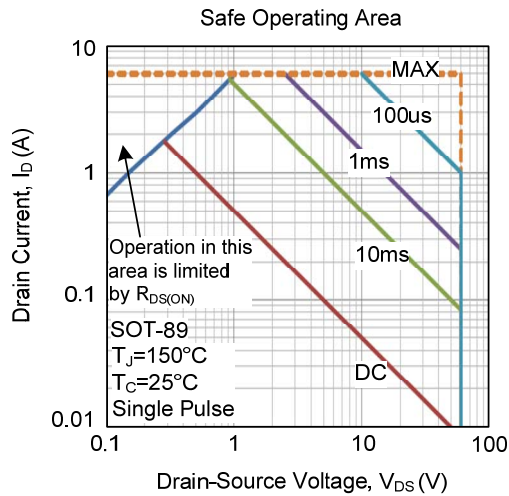
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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